Compal Confidential

Broadwell M/B Schematics Document

Intel ULV Processor with DDRIIIL

Date : 2015/01/31

BDL50 LA-D703P

Version 1.0

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Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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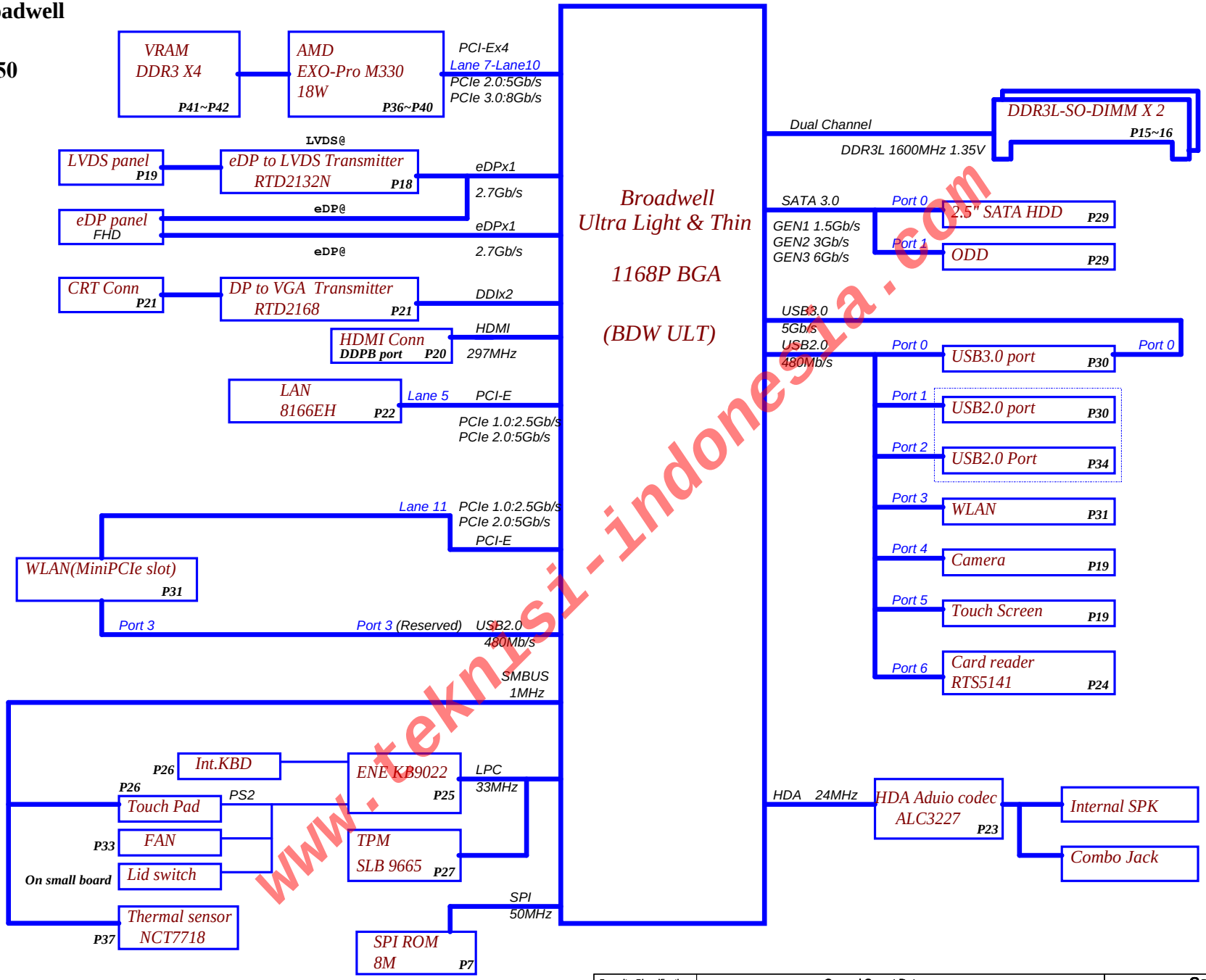
Title	Cover Page	
Size B	Document Number LA-D703P	Rev 0.1
Date: Saturday, January 31, 2015	Sheet 1 of 61	

Compal Confidential
Model Name : Broadwell

File Name : BDL50
LA-D703P



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Title: Block Diagrams

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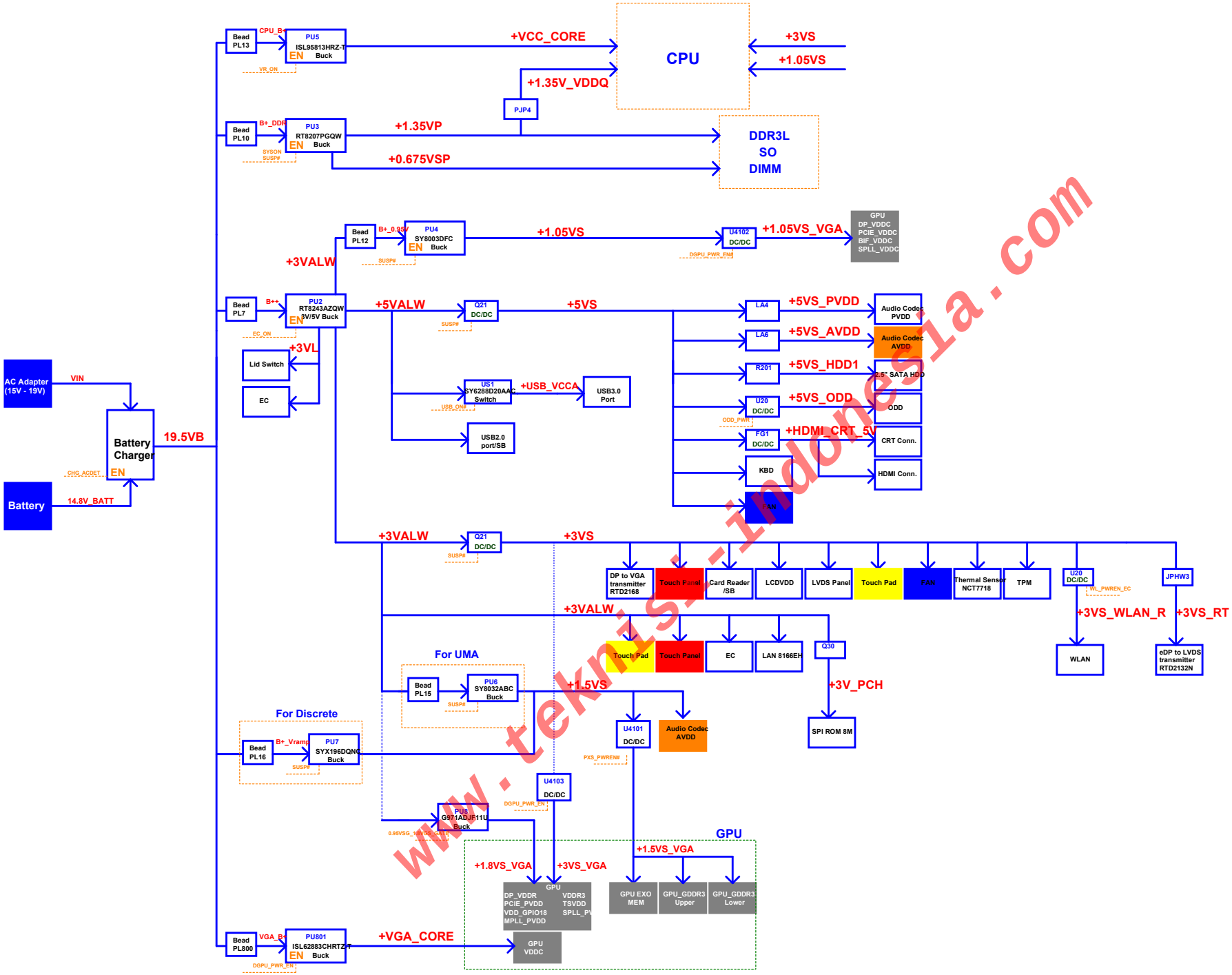
Date: Saturday, January 31, 2015 | Sheet 2 of 61



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Issued Date	2013/01/11	Deciphered Date 2015/04/22	Title System Power Tree
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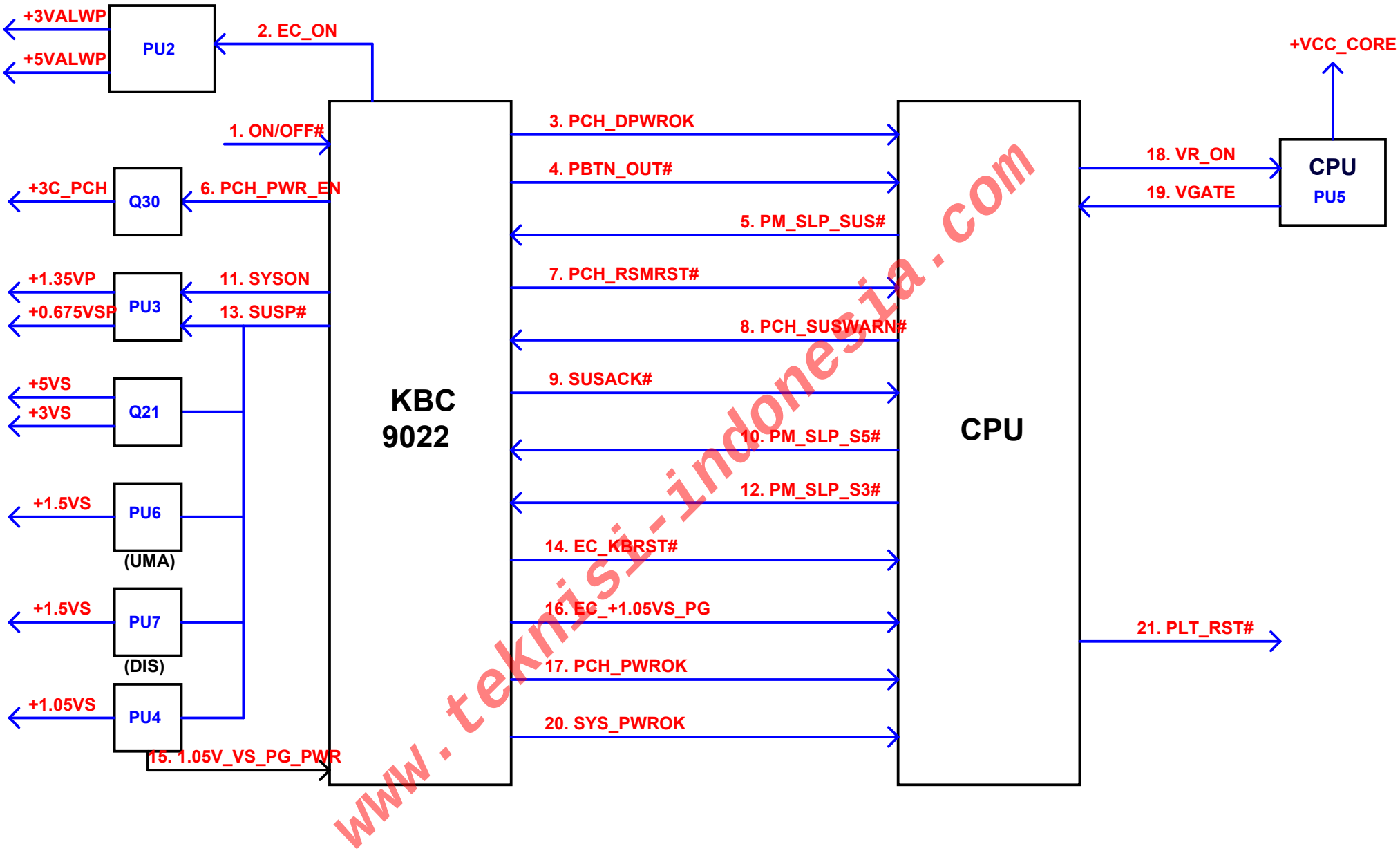
			Date: Sunday, January 31, 2013 Sheet 3 of 40



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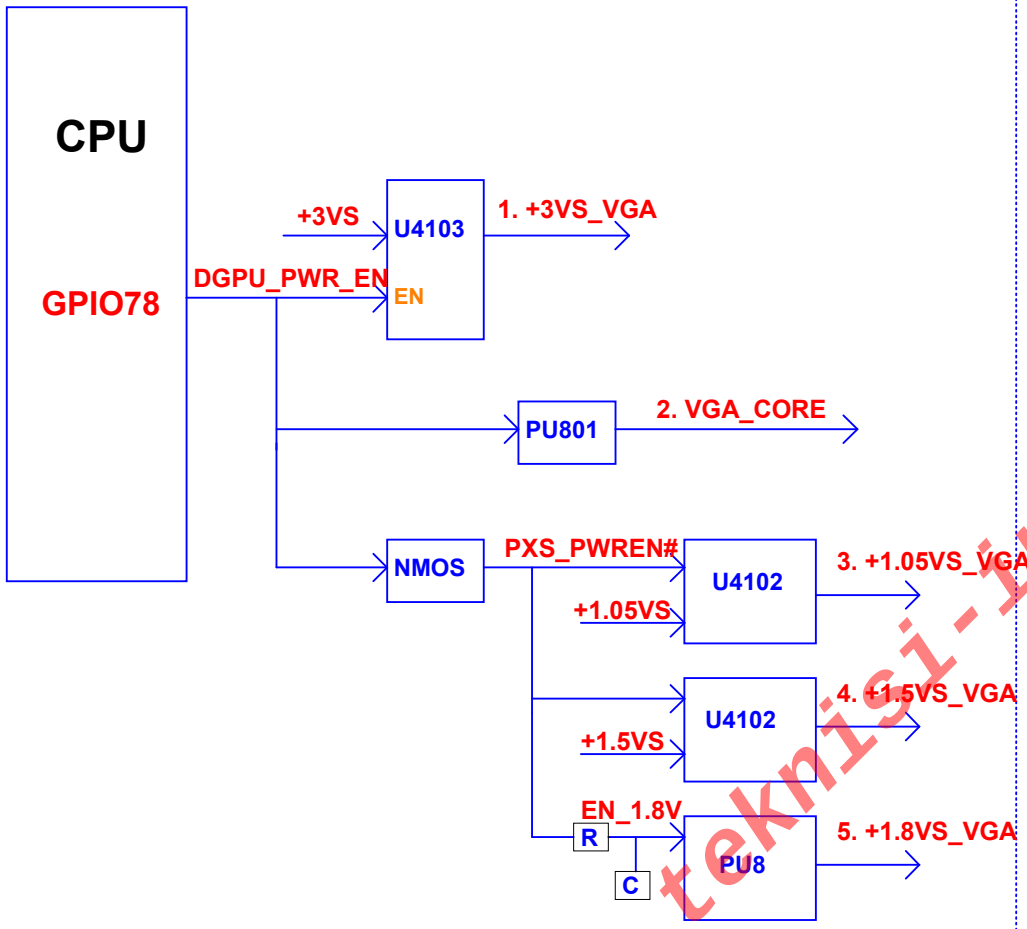
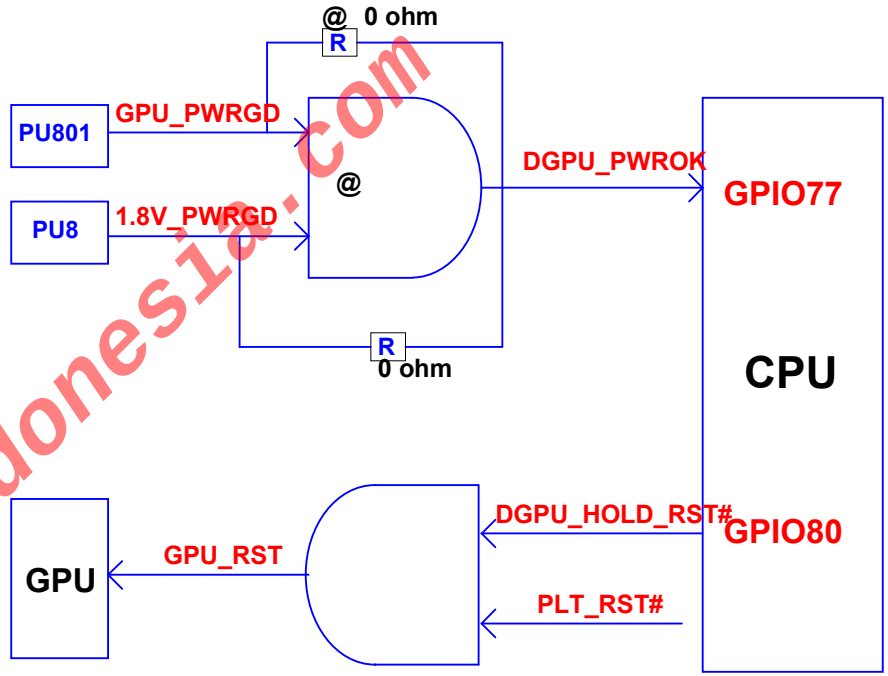
			Date: Saturday, January 31, 2015; Sheet 43 of 61





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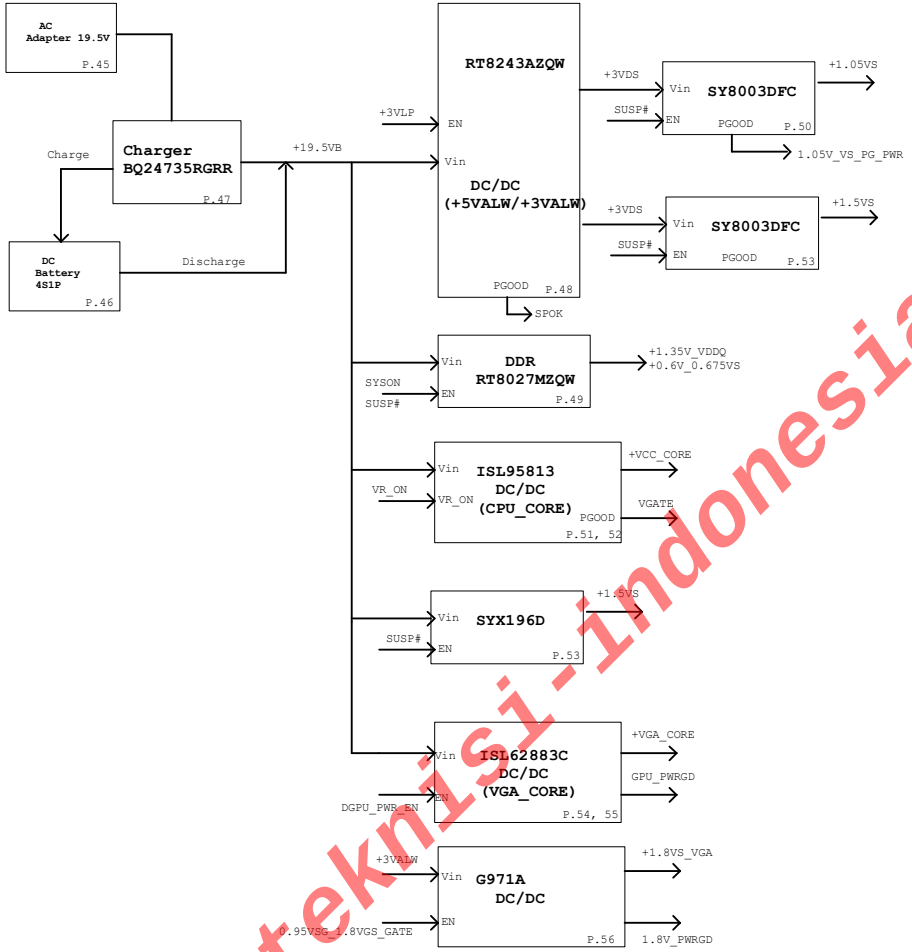
			Date: Saturday, January 31, 2015; Sheet 42 of 51



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Issued Date	2012/04/03	Deciphered Date	2014/12/31	Title: Power Block Diagram
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				Date: Saturday, January 31, 2015; Sheet 57 of 60

Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.35V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.675VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

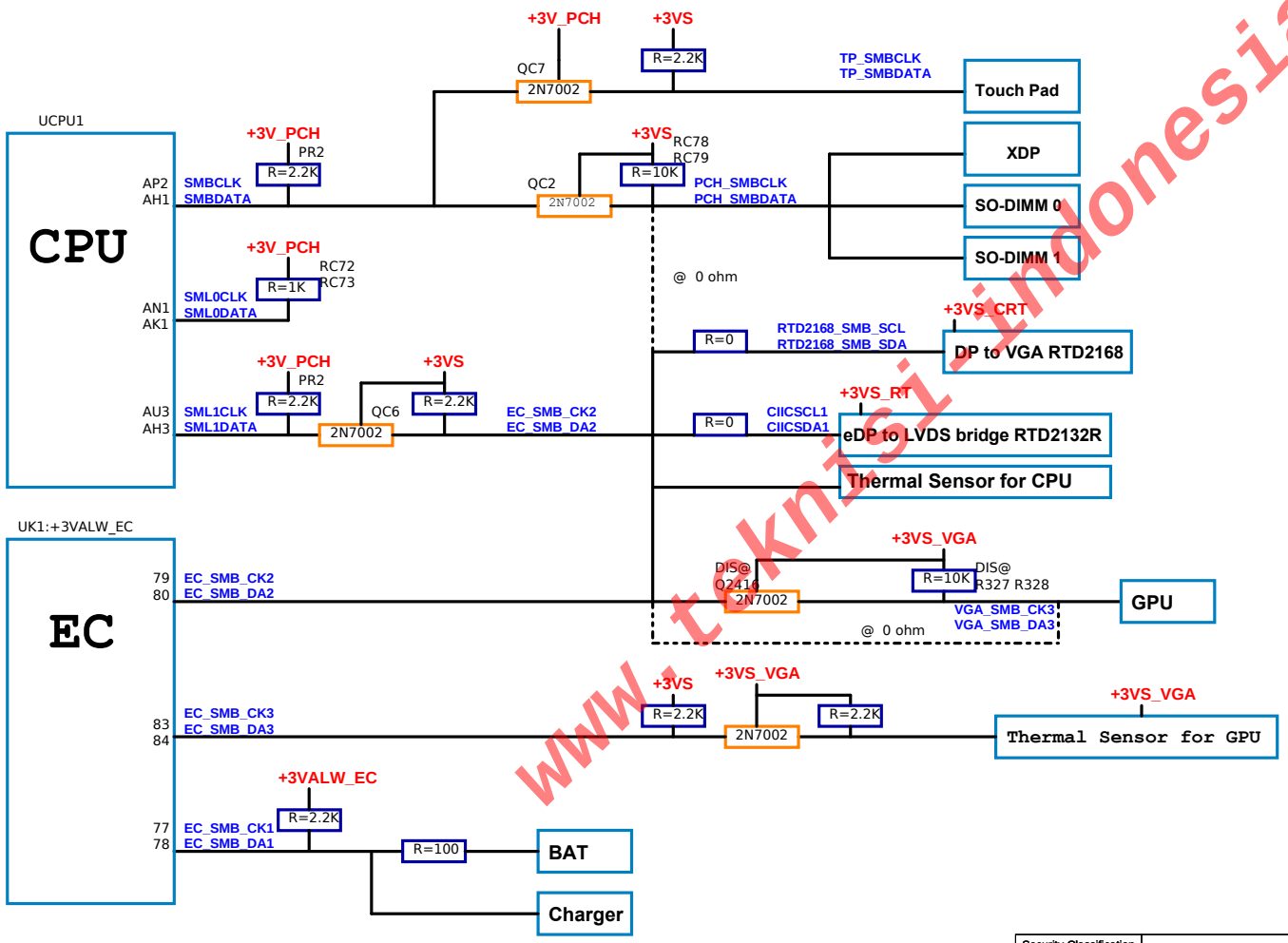
@ is NO SMT part (empty)

@EMI@,@ESD@,@RF@ : Reserve , don't pop.

RF@ : RF team request, must add.
EMI@ : EMI team request, must add.
ESD@ : ESD team request, must add.

SPI@ : SPI ROM request
LVDS@ : Support LVDS panel.
eDP@ : Support eDP panel

DIS@ : for AMD EXO
UMA@ : for UMA only
TP@ : TP SMBus
XTAL@ : for HSW SMT in DB phase only
GCLK@ : Support GCLK
GCLKUMA@ : UMA
GCLKDIS@: DIS
8111@ : for LAN giga
8166@ : for LAN 10/100



<USB2.0 port>

USB2.0 port	DESTINATION	
	UMA	Dis
0	USB 2.0/3.0(left side)	USB 2.0/3.0(left side)
1	USB 2.0(left side)	USB 2.0(left side)
2	USB 2.0(right side)	USB 2.0(right side)
3	WLAN/BT	WLAN/BT
4	Camera	Camera
5	Touch screen	Touch screen
6	Card reader	Card reader
7	X	X

<PCI-E,SATA,USB3.0>

Lane#	USB3.0	DESTINATION	
		UMA	Dis
0		USB3.0	USB3.0
1			

Lane#	PCIE	DESTINATION	
		UMA	Dis
0			
1			
2			
3		LAN	LAN

Lane#	SATA	DESTINATION	
		UMA	Dis
0		HDD	HDD
1		ODD	ODD
2		WLAN	WLAN

Lane#	PEG	DESTINATION	
		UMA	Dis
0			GPU
1			
2			
3			

Lane#	PCIE REQ	DESTINATION	
		UMA	Dis
0		LAN	LAN
1		X	X
2		WLAN	WLAN
3		X	GPU
4		PU	PU
5		PU	PU

Board ID control

15"	DB	SI	PV	MV
UMA RK4	0 ohm	15K ohm	27K ohm	43K ohm
DIS RK4	12k ohm	20k ohm	33k ohm	56k ohm

Thermal Sensor

CPU internal : PECI protocal
PCH internal : 0x90
GPU internal : 0x82
CPU external : 0x98
GPU external : 0x98

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Title: Notes List

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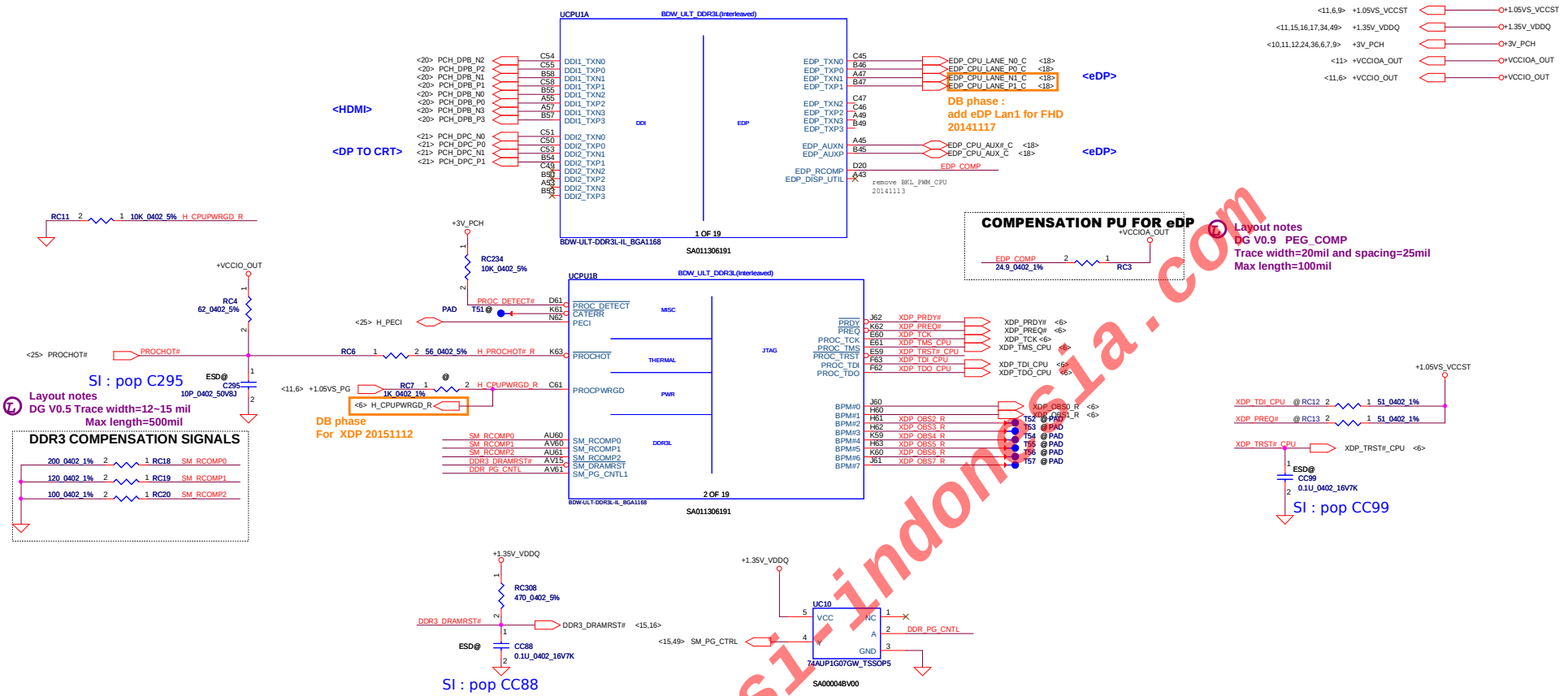

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Title: DDI,MSIC,XDP

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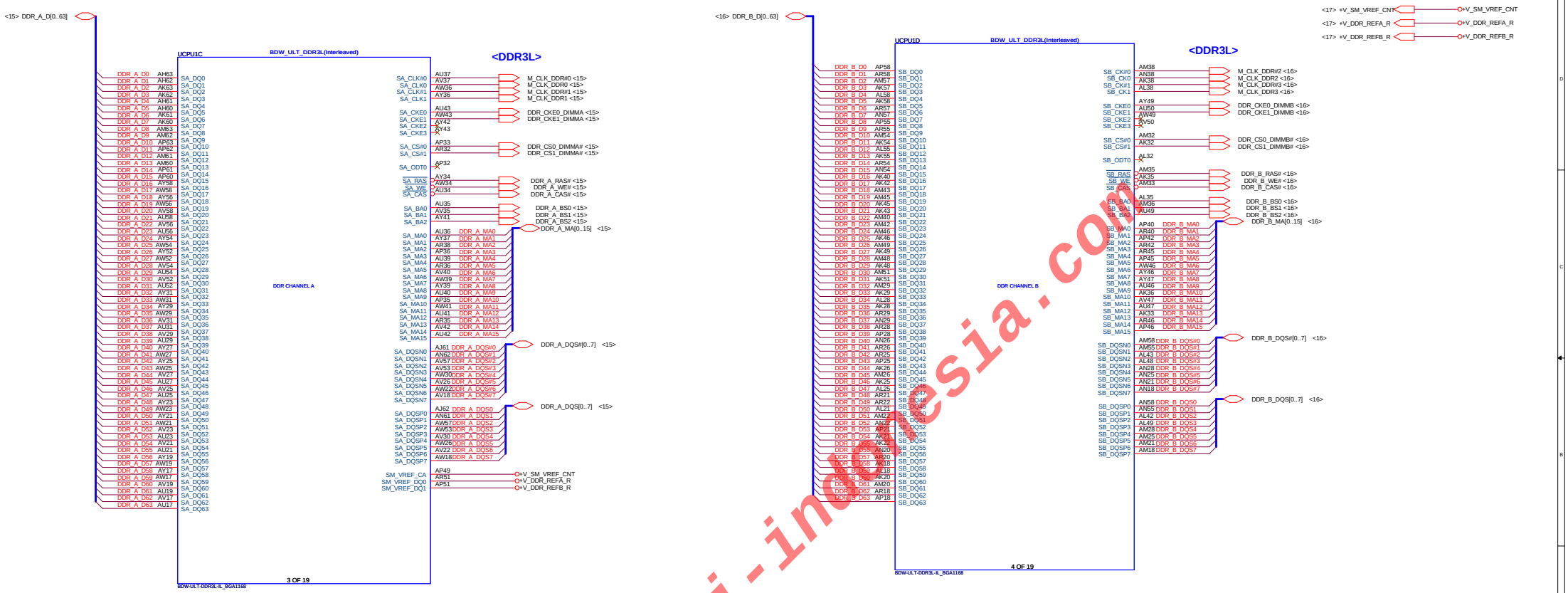

Interleaved Memory

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Compal Electronics, Inc.

Title: DDRIII

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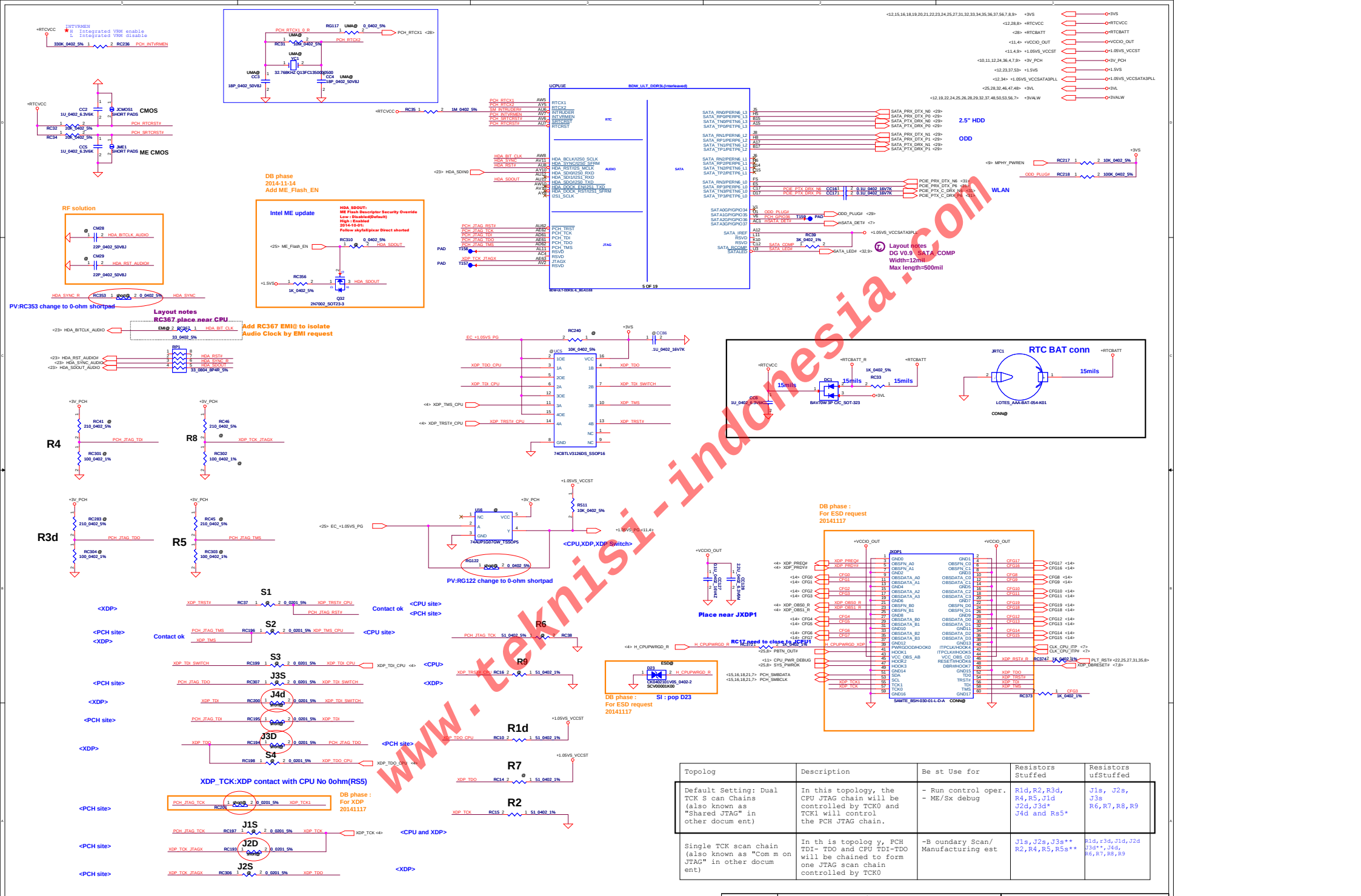

Topolog	Description	Be st Use for	Resistors Stuffed	Resistors ufStuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other docum ent)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1d,R2,R3d, R4,R5,J1d J2d,J3d* J4d and Rs5*	J1s, J2s, J3s R6,R7,R8,R9
Single TCK scan chain (also known as "Com m on JTAG" in other docum ent)	In th is topolog y, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-B oundary Scan/ Manufacturing est	J1s,J2s,J3s** R2,R4,R5,R5s**	R1d,r3d,J1d,J2d J3d**,J4d, R6,R7,R8,R9

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Title: RTC,SATA,HDA,JTAG

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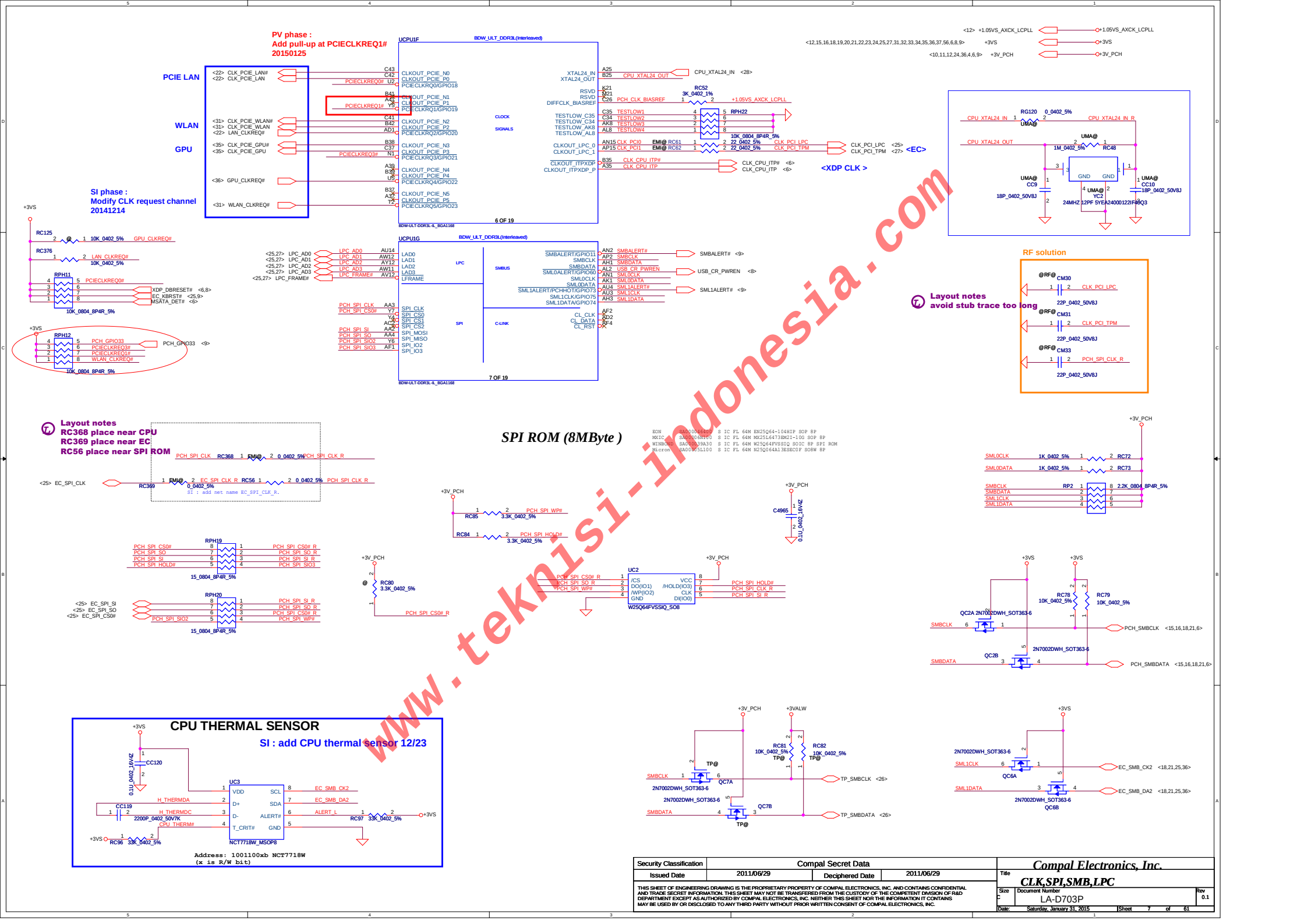

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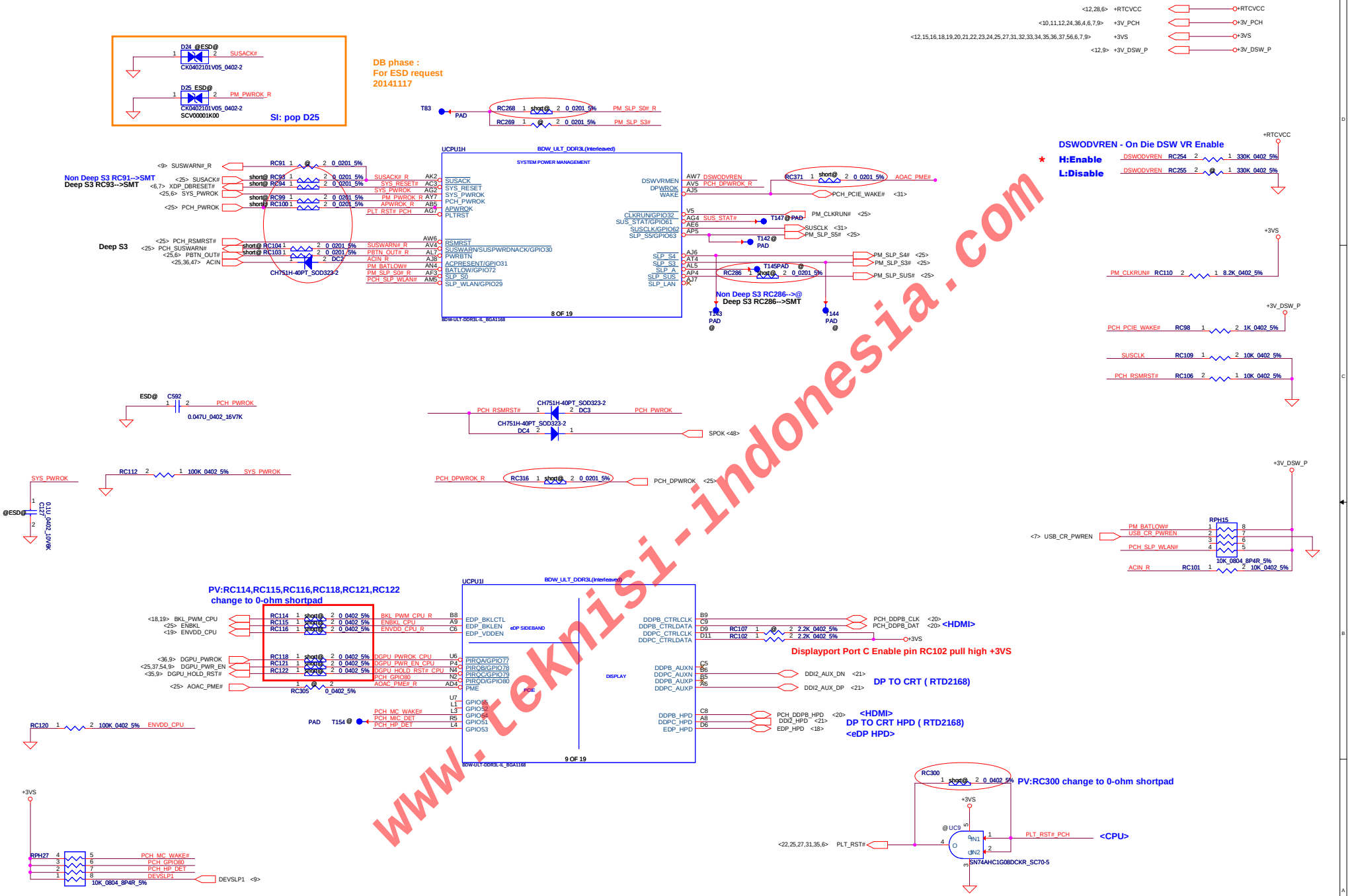

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Title: PM,GPIO,DDI

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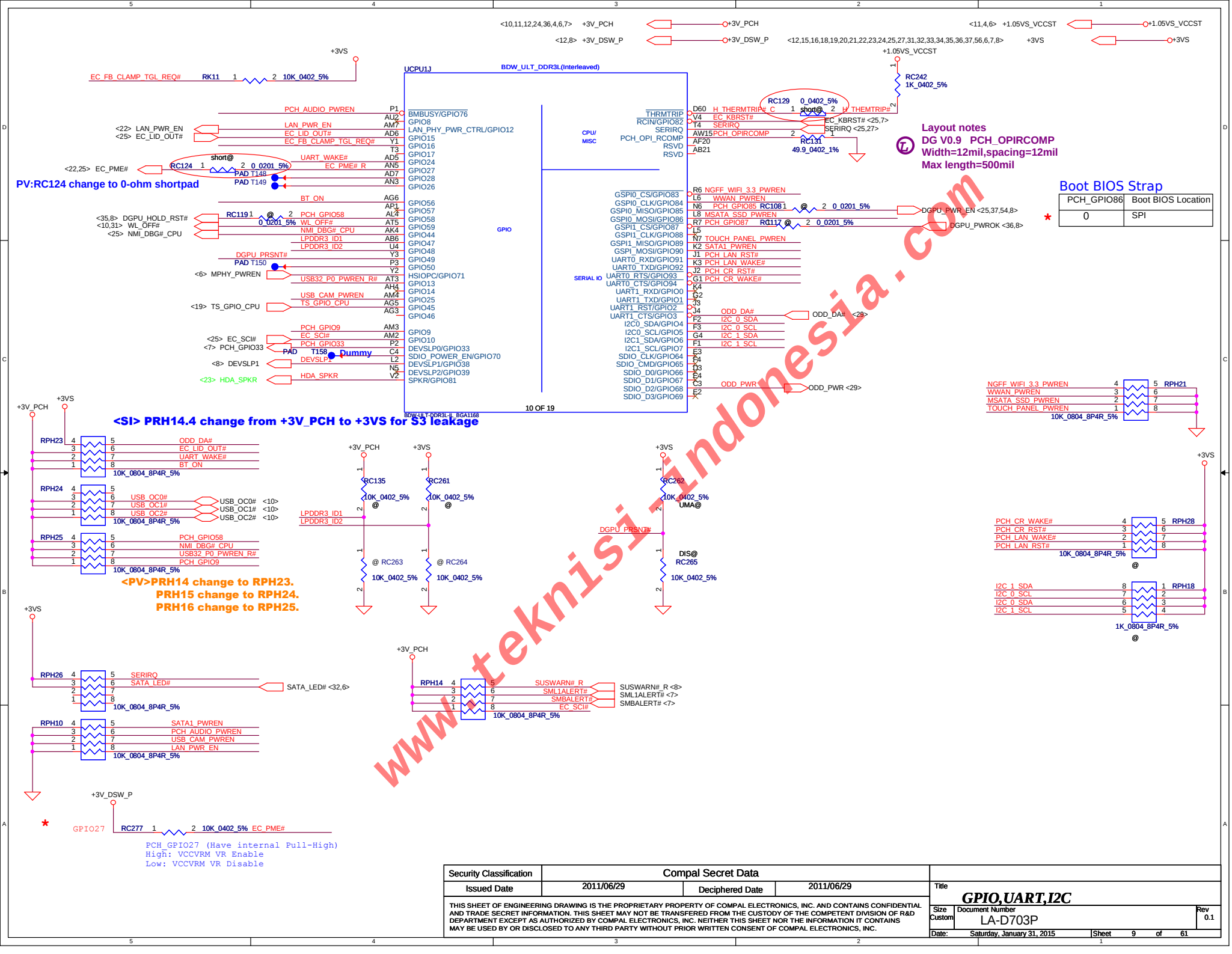

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Title: **GPIO,UART,I2C**

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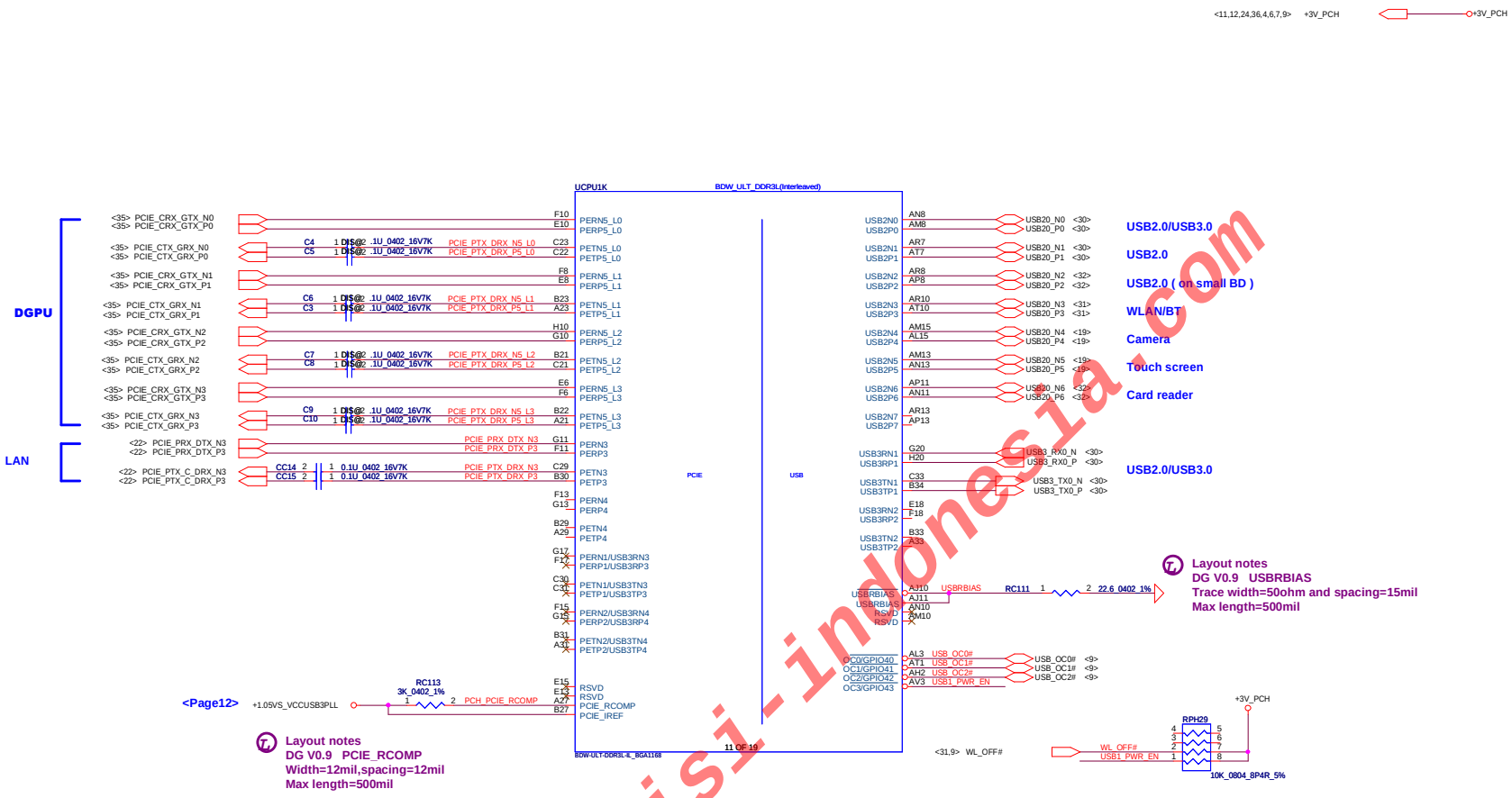

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Title: **PCIE,USB**

Size: C | Document Number: LA-D703P | Rev: 0.1

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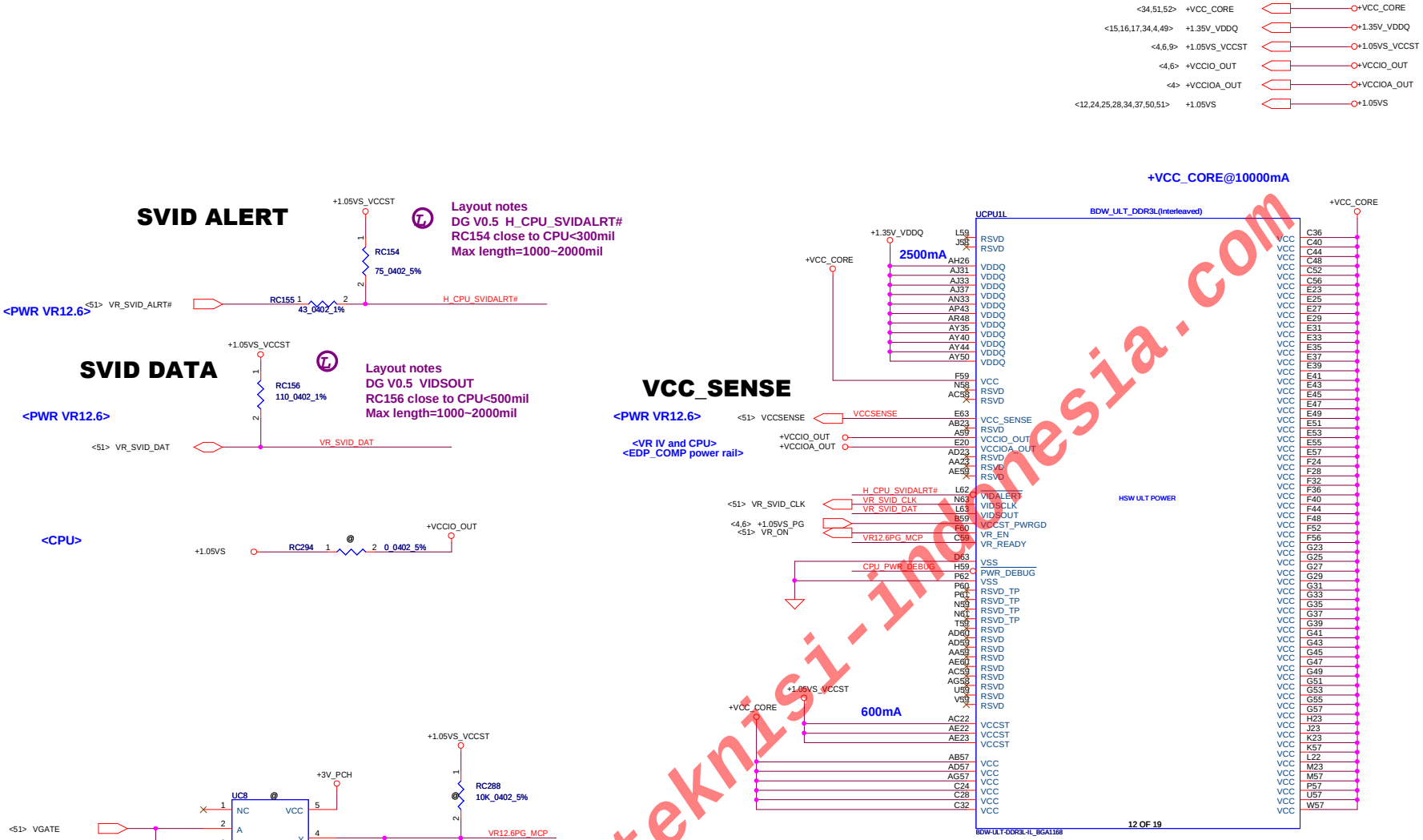

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Title: **Power**

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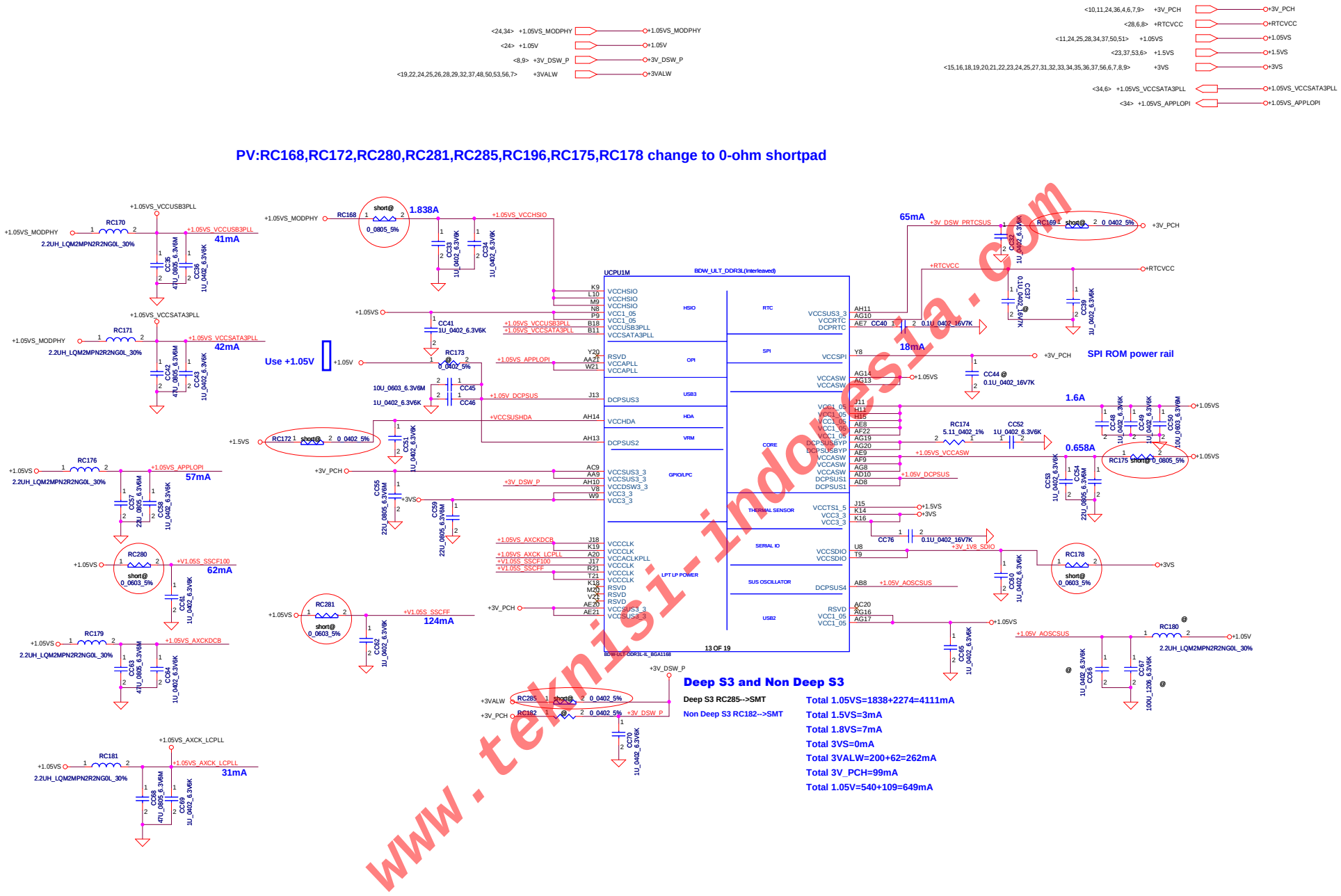
Date: Saturday, January 31, 2015 | Sheet 11 of 61



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Title: **Power**

Size	Document Number	Rev
C	LA-D703P	0.1

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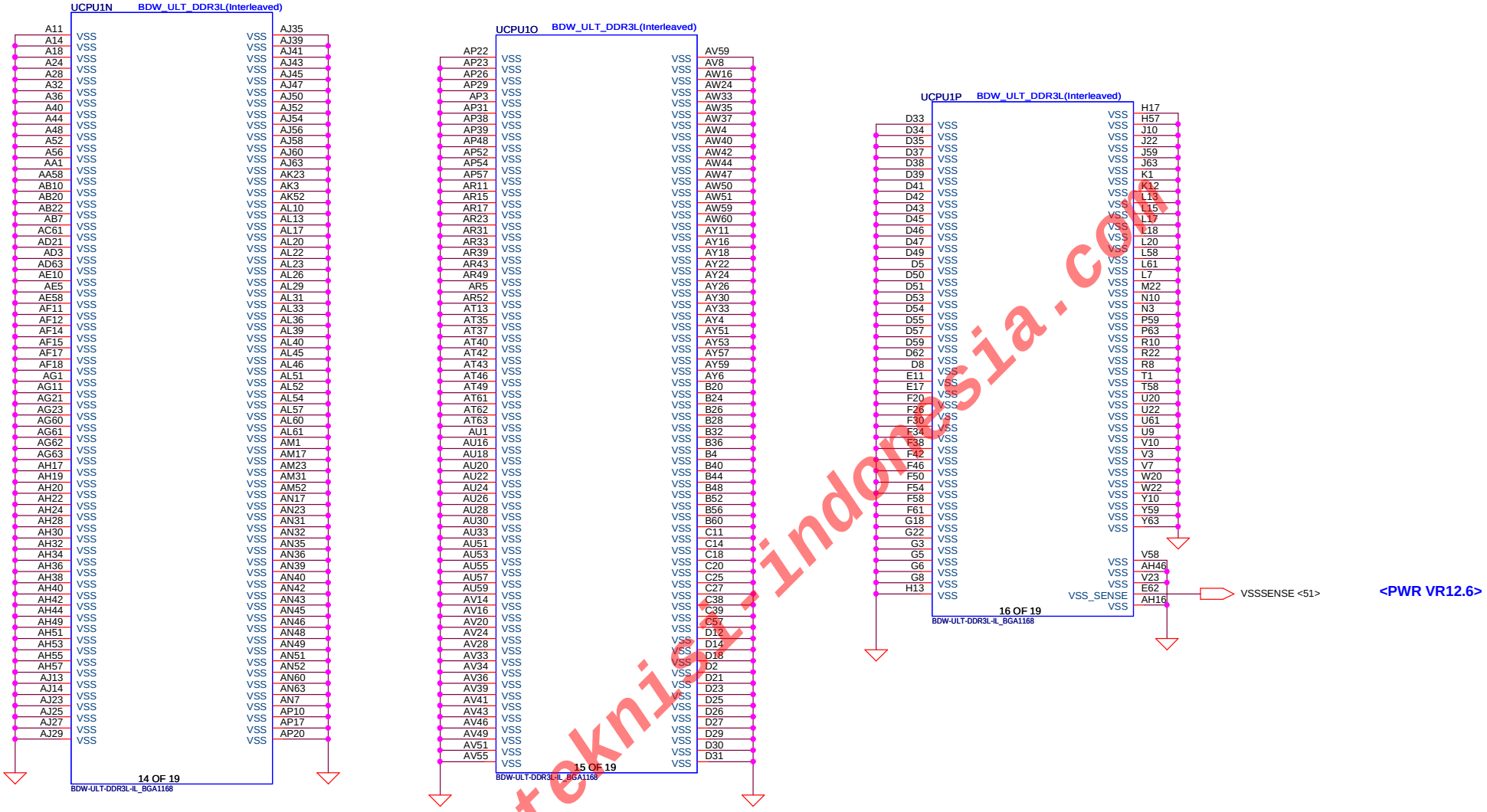

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Title: GND/VSSSEN

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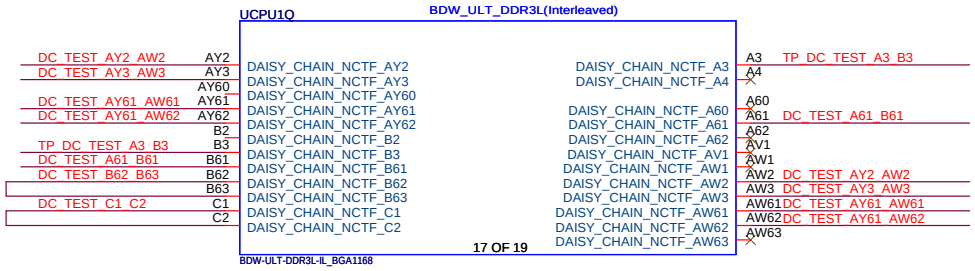
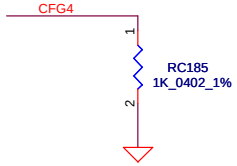
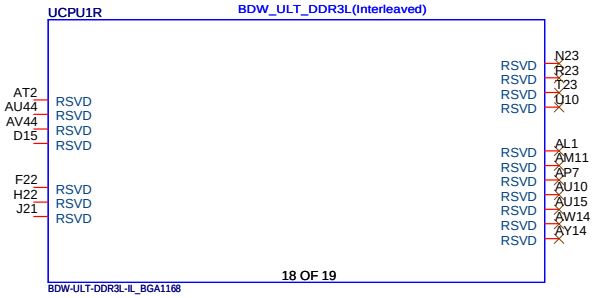
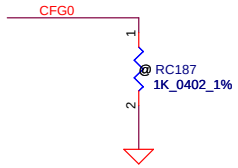
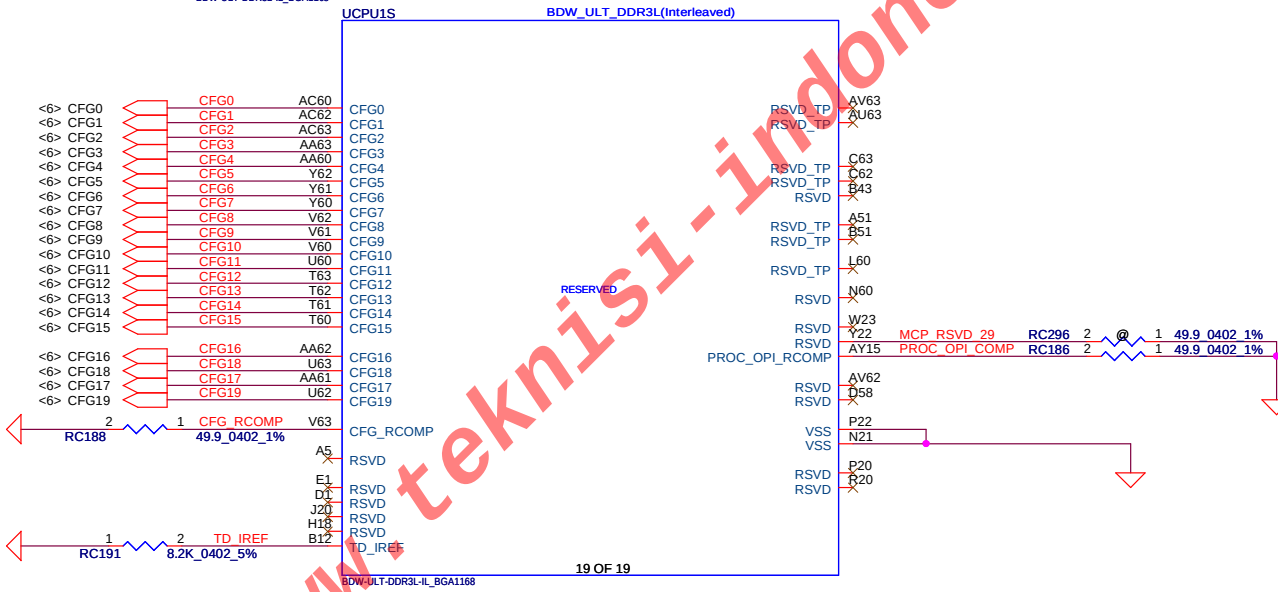




Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port







Layout notes
DG V0.9 PROC_OPI_COMP
Width=12mil,spacing=12mil
Max length=500mil

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Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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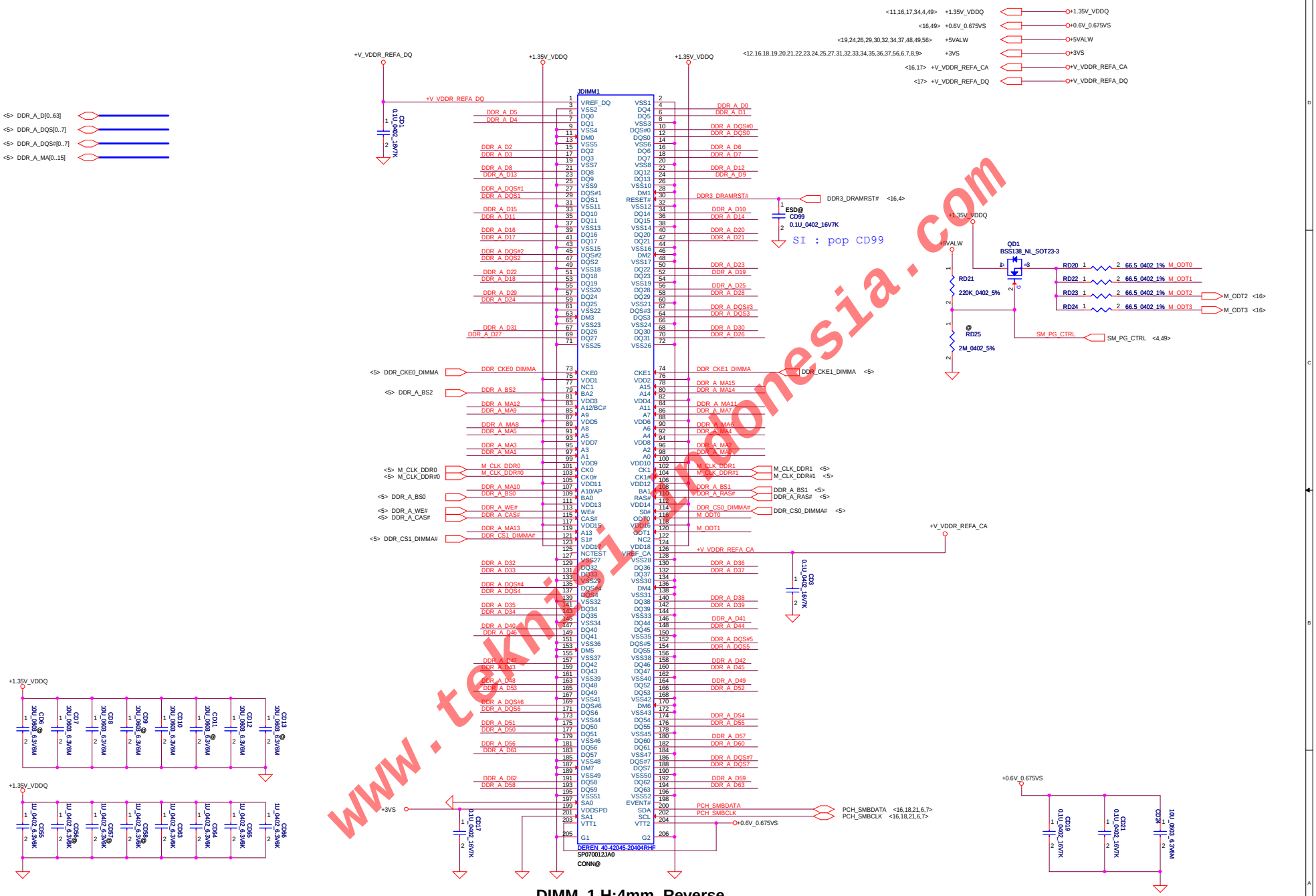
Compal Electronics, Inc.

Title: **RSVD/CFG**

Size	Document Number	Rev
	LA-D703P	0.1

Date: Saturday, January 31, 2015 | Sheet 14 of 61



DIMM_1 H:4mm Reverse

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Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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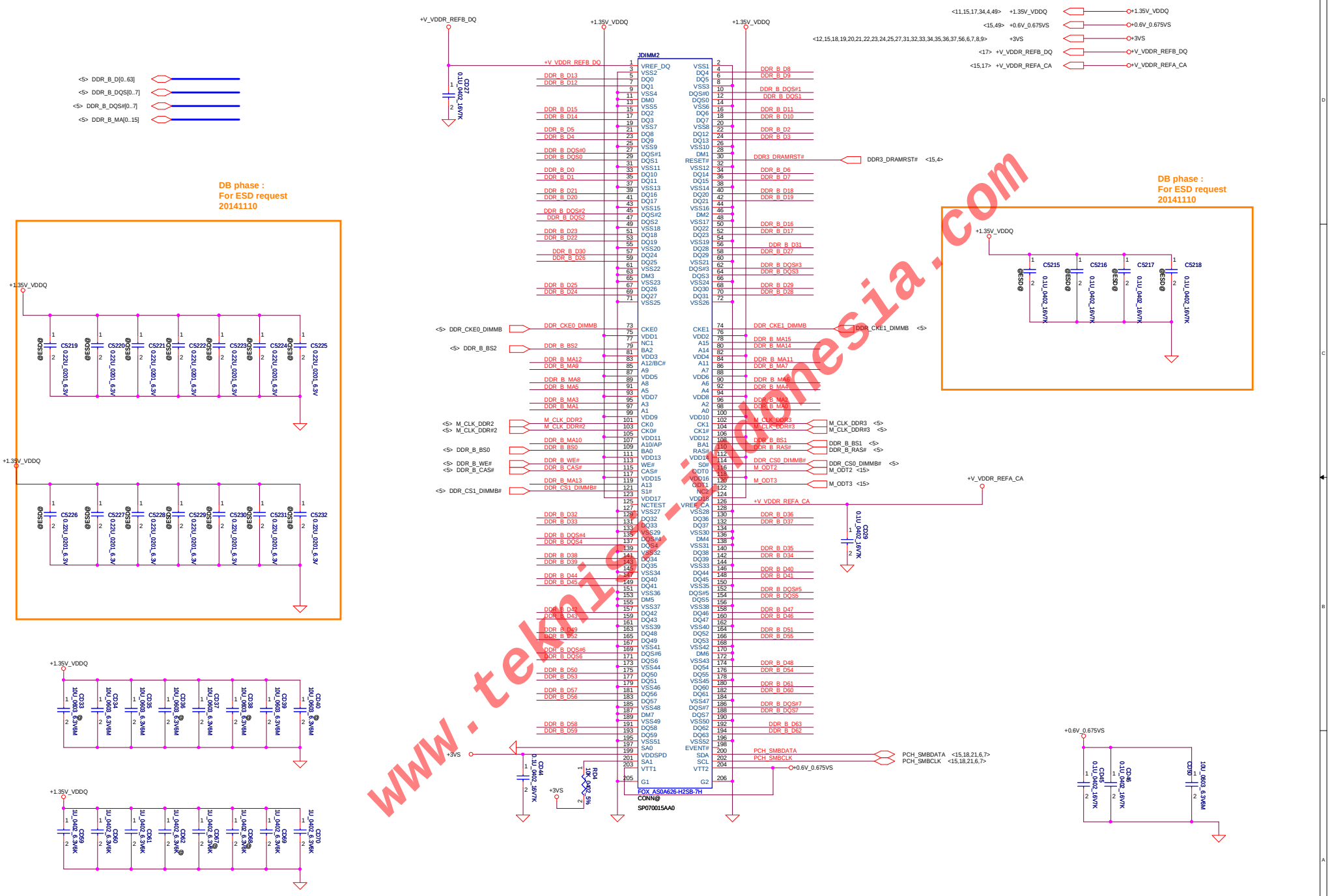
Title: **DDR3L DIMM0**

Size	Document Number	Rev
C	LA-D703P	0.1

Date: Saturday, January 31, 2015 | Sheet 15 of 61



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Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

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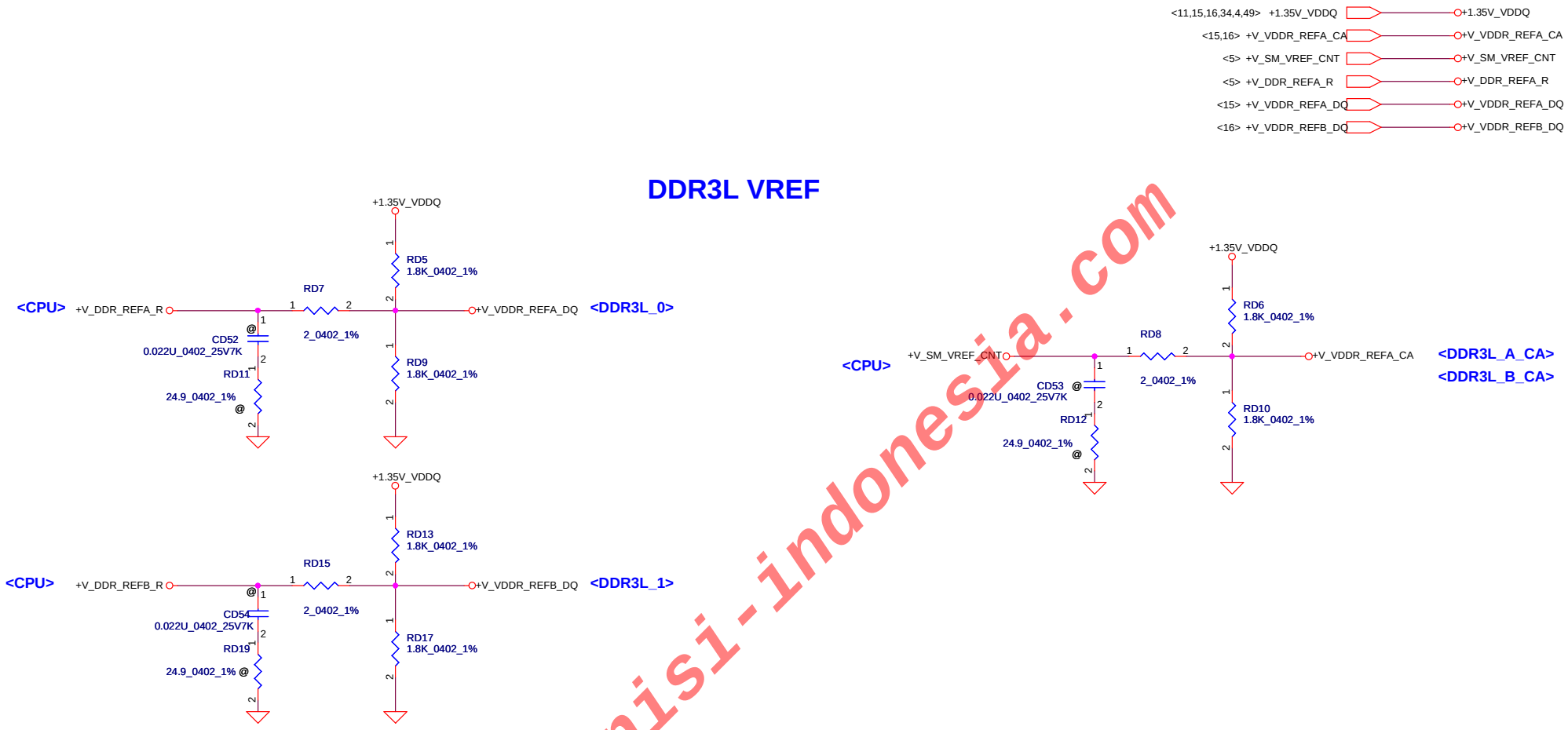
Compal Electronics, Inc.

Title: DDR3L DIMM1

Size	Document Number	Rev
	LA-D703P	0.1

Date: Saturday, January 31, 2015 | Sheet 16 of 61



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Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title: DDR3L VREF
				Size: Document Number: LA-D703P Rev: 0.1
				Date: Saturday, January 31, 2015 Sheet 17 of 61

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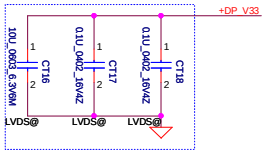
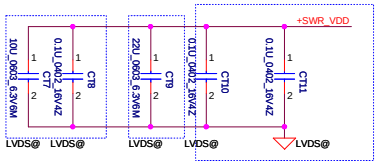
JPHW3 need to short

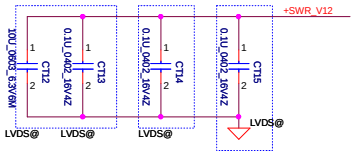
Layout notes
CT16~CT18 Close to Pin3



Layout notes
Close to LT5 Pin18 Pin13

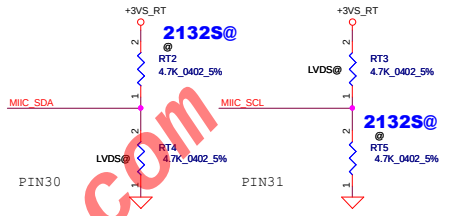


Layout notes
Close to Pin11 Pin27 Pin7



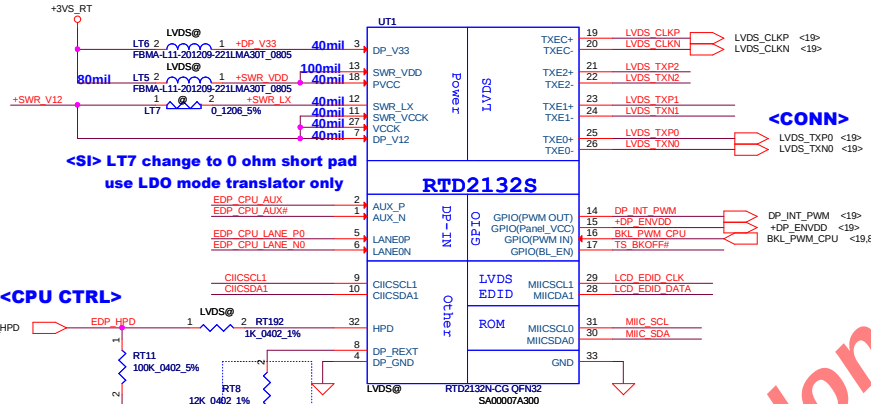
ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

Default mode



SWR / LDO Mode select

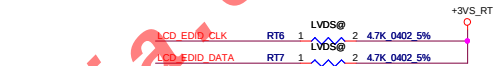
	LDO	SWR
2132S	Do not support	mount LT7
2132N	Use 0 ohm	mount LT7
If use 2132N, please select LDO mode as default.		



<SI> LT7 change to 0 ohm short pad use LDO mode translator only

<CONN>

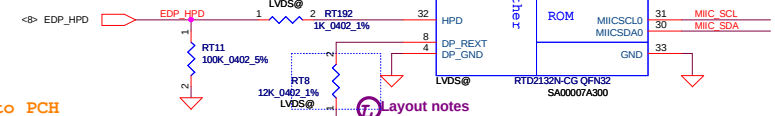
<CONN> <CPU>



	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *
* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm	

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V
* Version R has internal level shifter, remove level shifter circuit on AMD platform	

<CPU CTRL>

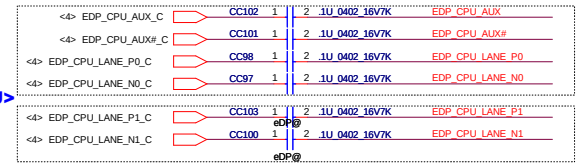


Layout notes
RT8 close to pin8

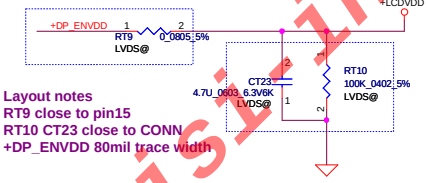
RTD2132 SMBus revrse to PCH

Layout notes
CC97~CC102 must closed to connector

<CPU>



DB phase :
add eDP Lan1 for FHD
20141117

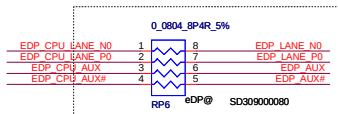


Layout notes
RT9 close to pin15
RT10 CT23 close to CONN
+DP_ENVDD 80mil trace width

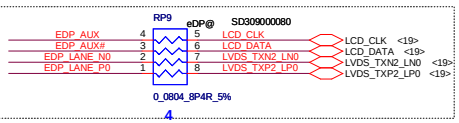
Different between 2132S and 2132R

2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

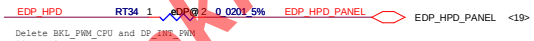
<CPU by PASS eDP>



<eDP to connector>



Layout notes
RP6 RP9 RP10 must closed to connector

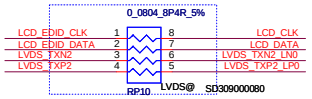


Delete BKL_PWM_CPU and DP_INT_PWM
20141113

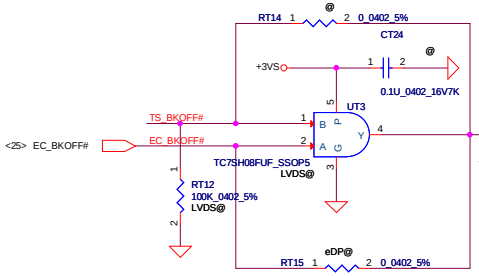
DB phase :
add eDP Lan1 for FHD
20141117

Layout notes
RT16~RT19 must closed to connector

<LVDS to connector>



<RTS2132>
<EC CTRL>



<LVDS Panel>

PD 100K on LVDS page

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Issued Date	2013/3/1	Deciphered Date	2015/3/1

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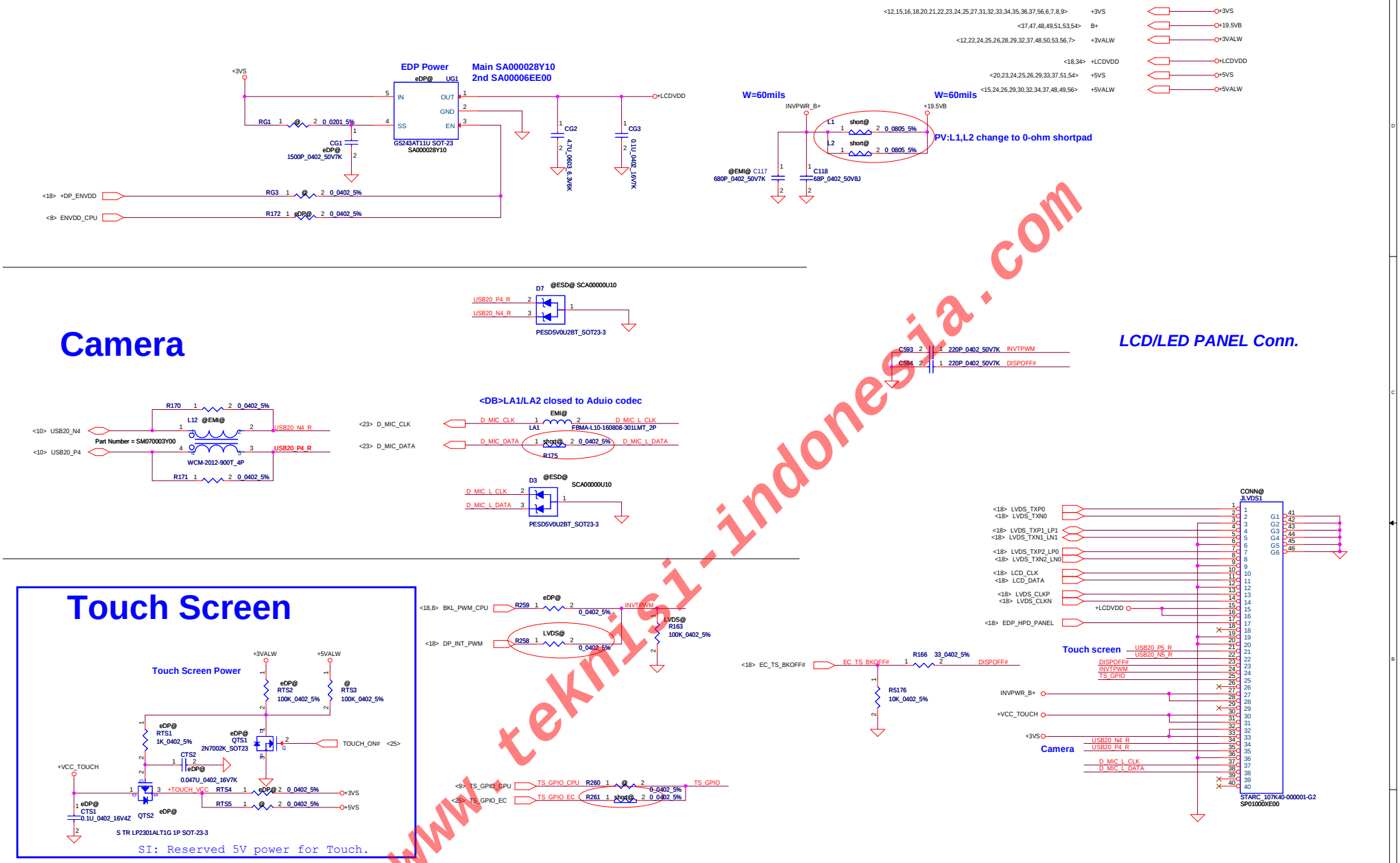
Compal Electronics, Inc.

Title: *LVDS Translator-RTD2132N*

Size | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 18 of 61



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Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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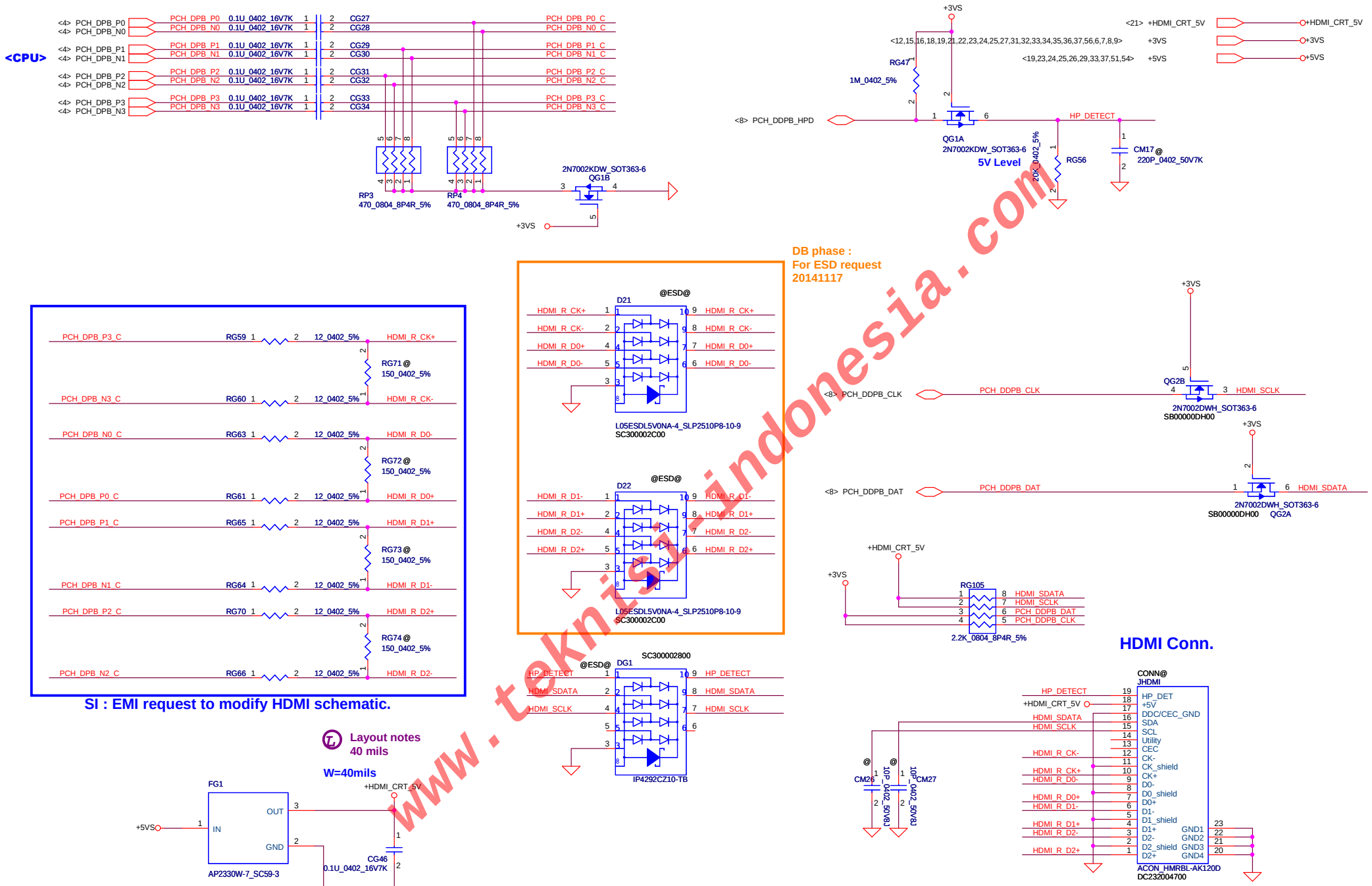
Compal Electronics, Inc.

Title: **LVDS Connector**

Size: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 19 of 61



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Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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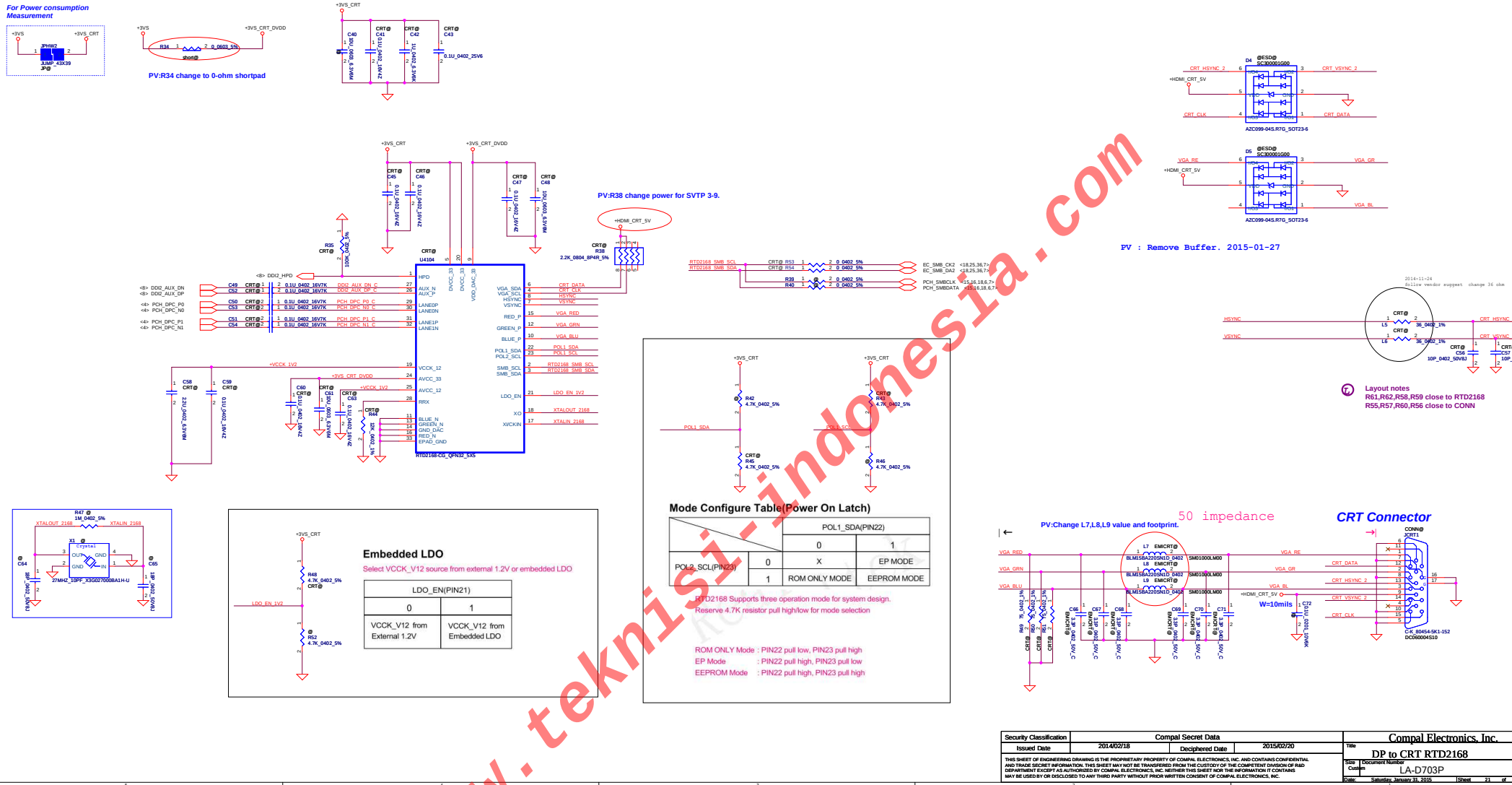
Compal Electronics, Inc.

Title: **HDMI Conn/Level shift**

Size | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 20 of 61

DP to CRT converter



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Security Classification	Compal Secret Data		
Issued Date	2014/02/18	Deciphered Date	2015/02/20

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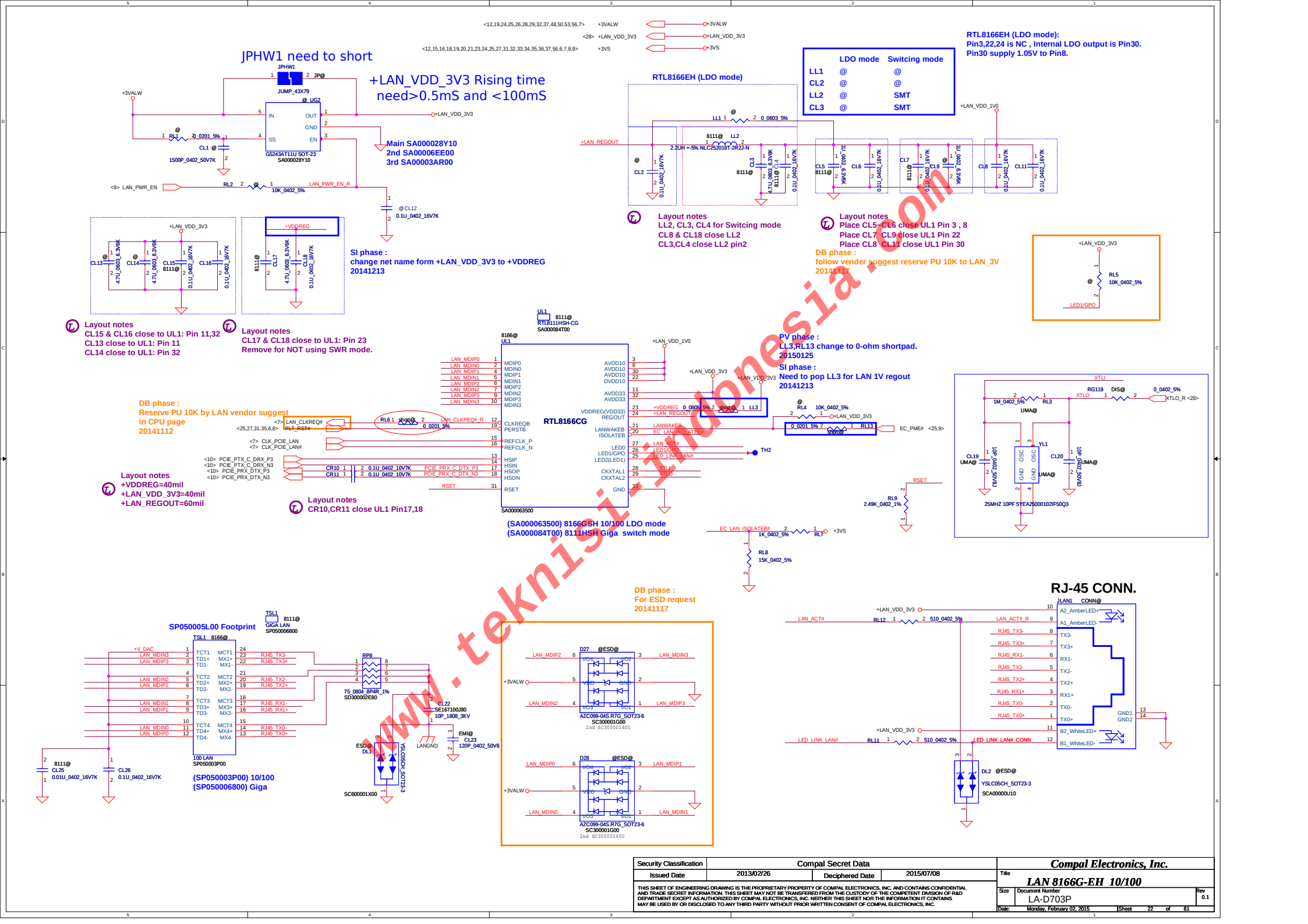
Compal Electronics, Inc.

Title: DP to CRT RTD2168

Size: Custom | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 21 of 61



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Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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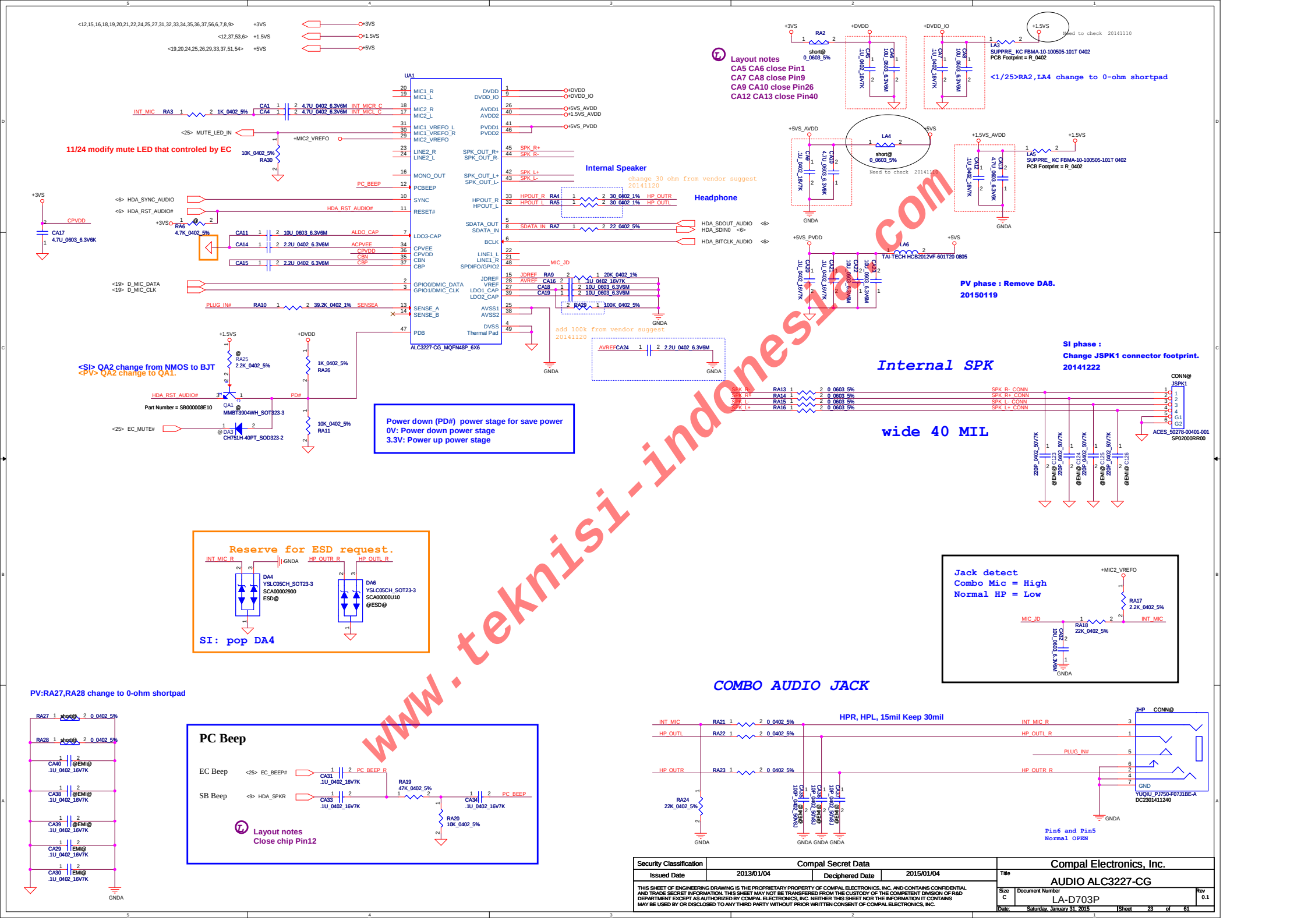
Compal Electronics, Inc.

Title: **LAN 8166G-EH 10/100**

Size	Document Number	Rev
	LA-D703P	0.1

Date: Monday, February 02, 2015 | Sheet 22 of 61



Security Classification	Compal Secret Data		
Issued Date	2013/01/04	Deciphered Date	2015/01/04

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Compal Electronics, Inc.

Title: AUDIO ALC3227-CG

Size: C | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 23 of 61

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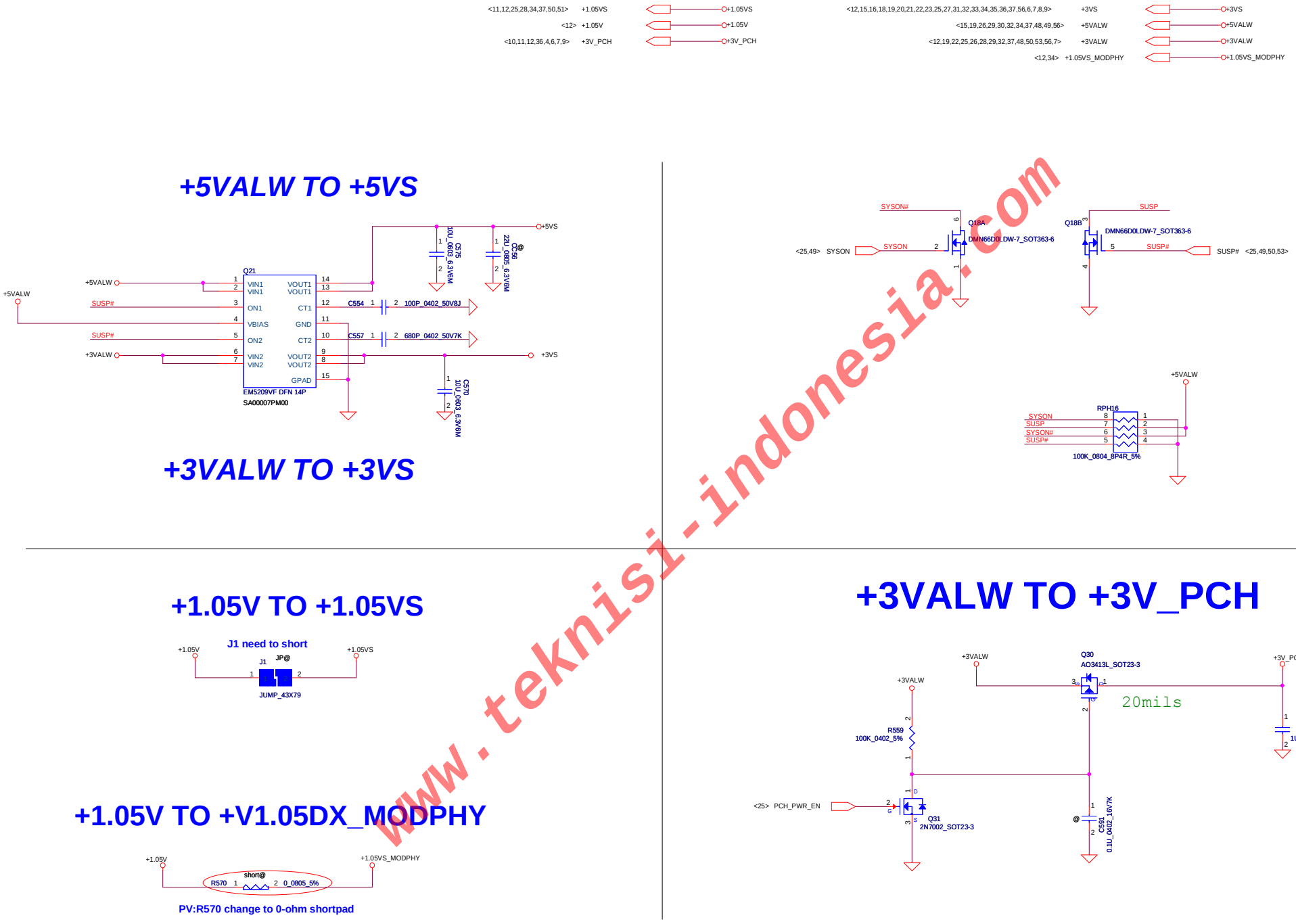

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Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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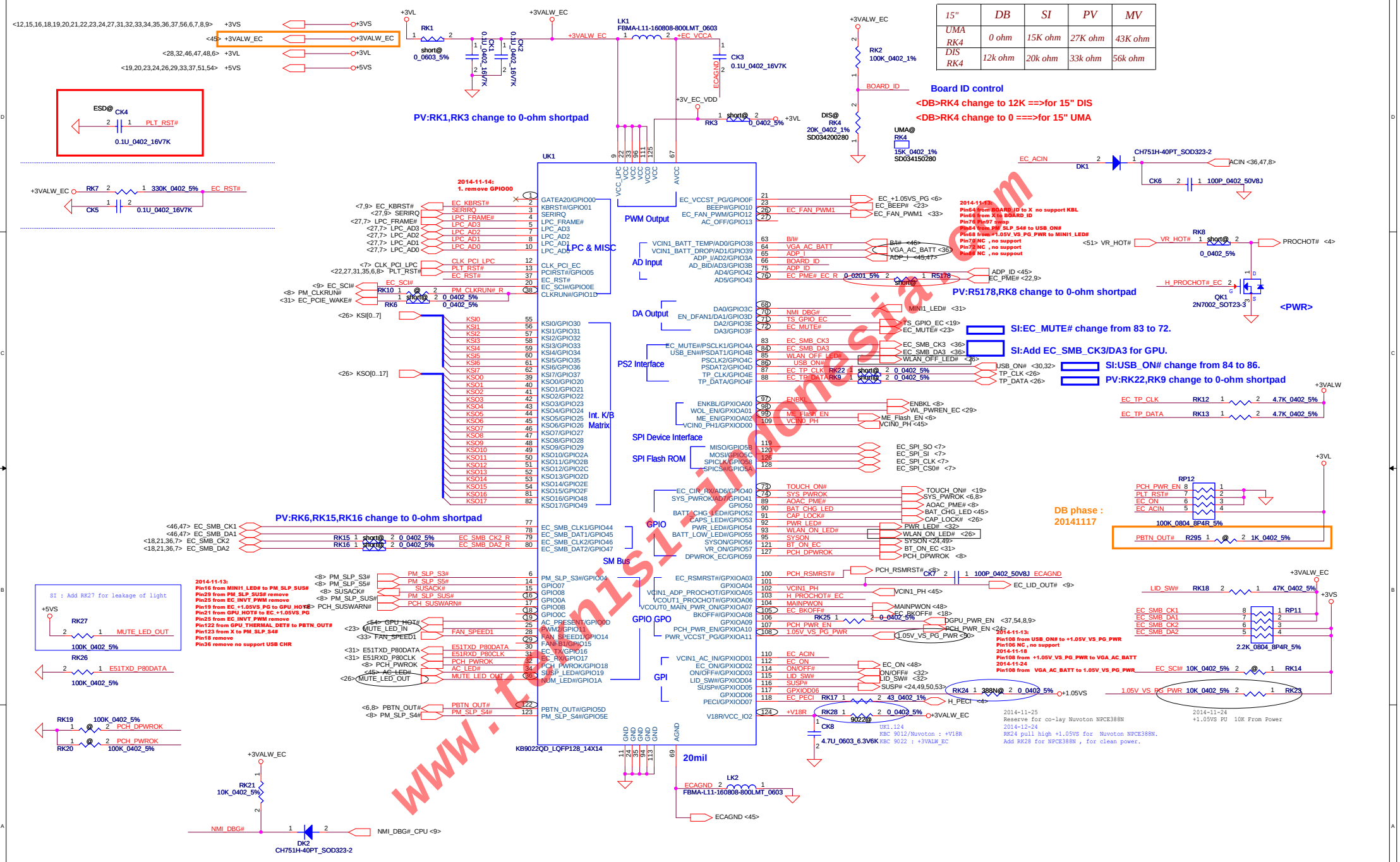
Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 24 of 61



15"	DB	SI	PV	MV
UMA RK4	0 ohm	15K ohm	27K ohm	43K ohm
DIS RK4	12k ohm	20k ohm	33k ohm	56k ohm

www.tunisi-indonesia.com

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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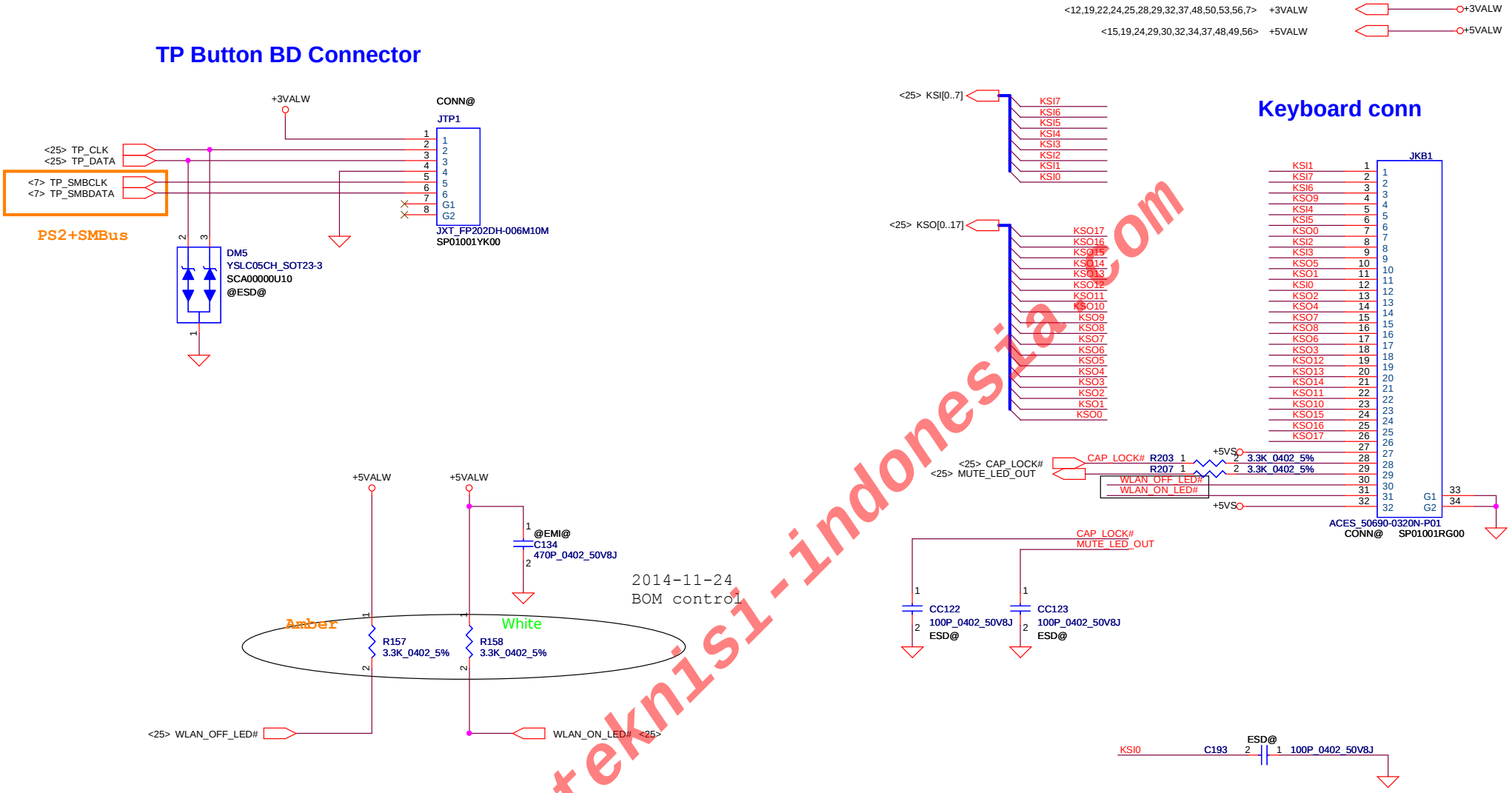
Compal Electronics, Inc.

Title: EC ENE-KB9022

Size: Custom | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 25 of 61



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Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

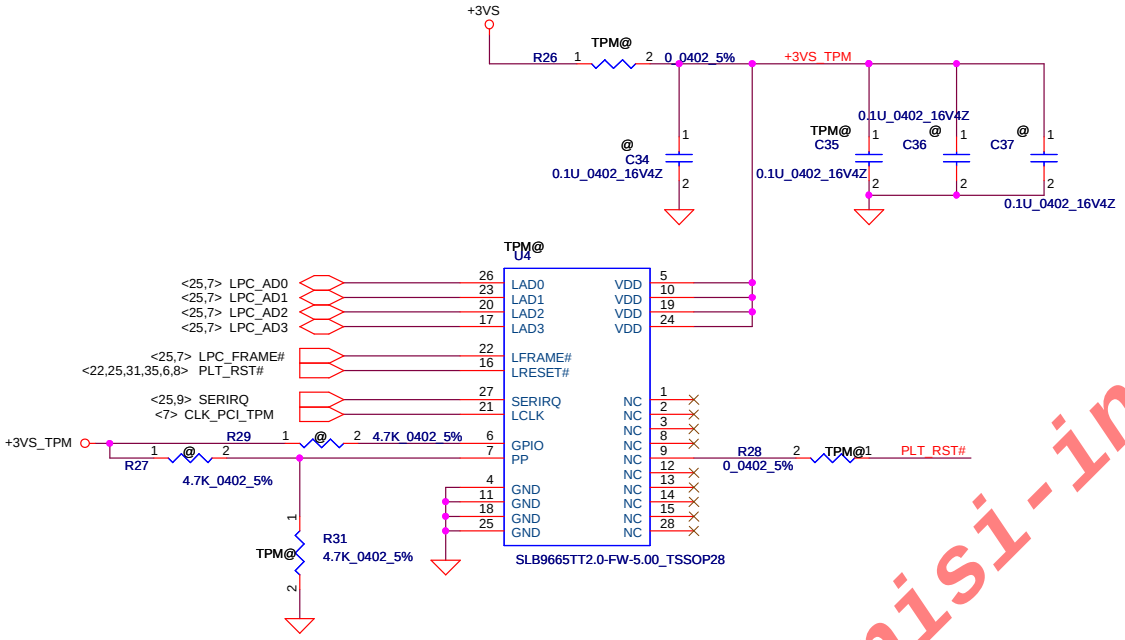
Title: KB/TP

Size: B | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 26 of 61

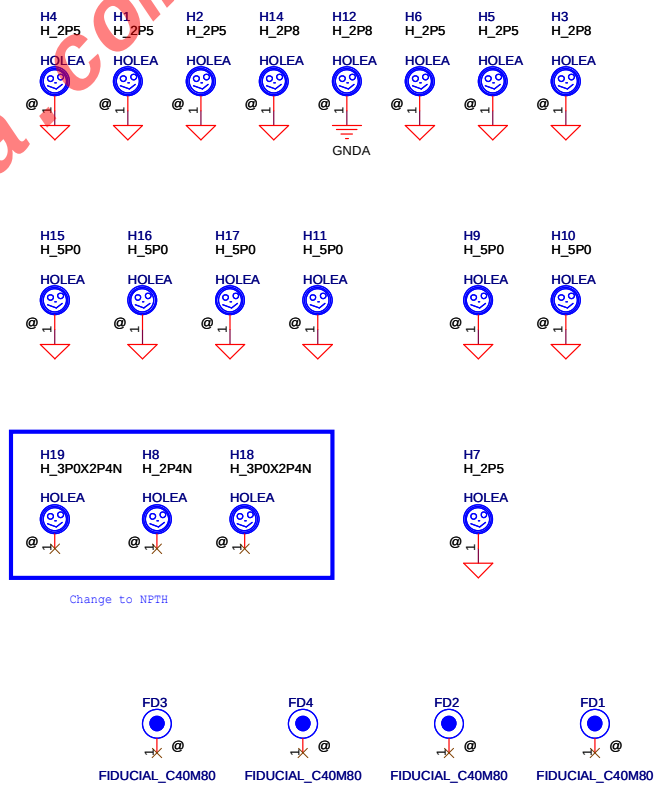
<12,15,16,18,19,20,21,22,23,24,25,31,32,33,34,35,36,37,56,6,7,8,9> +3VS

TPM2.0



SLB9665 (SA00007XU00)-->TPM2.0
SLB9660 (SA00007AB00) -->TPM1.2

Screw Hole



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Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: **TPM/Screw**

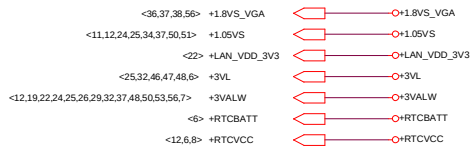
Size	Document Number	Rev
	LA-D703P	0.1

Date: Saturday, January 31, 2015 | Sheet 27 of 61

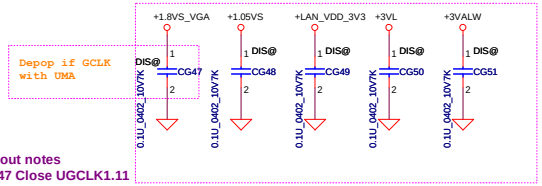
BOM control

Platform	Silego P/N	Compal PN	25MHz(A)	32.768KHz	24MHz(B)	27MHz	8MHz	Remark
Intel ULT UMA	SLG3NB3455VTR	SA00008IQ00	1	1	1	X	X	@
Intel ULT Dis	SLG3NB3456VTR	SA00008J800	1	1	1	1	X	DIS@

Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X'TAL use 10ppm.

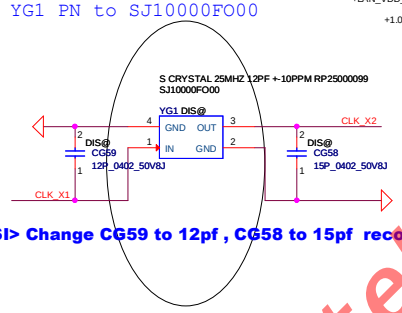


20141120 vendor recommend
1. AMD GPU power rail should be 1.8V, please modify +3VS_VGA to AMD GPU power rail.
2. CG47, CG48, CG49, CG50 and CG51 must placed close to UGCLK1.11, UGCLK1.3, UGCLK1.8, UGCLK1.15 and UGCLK1.2.
3. Please place RG114, RG109, RG111 and RG113 close to UGCLK1 for Impedance matching.
4. Modify RG114 Symbol from @ to GCLK@.
5. Change RG109 value from 33ohm to 10ohm.
6. We recommend to add RGxxx and RGyyy for isolated 32.768k and 24M clock tail.
7. We recommend to add CGxx, it is reserved for EMI.
8. We recommend to change CG54 Symbol from GCLK@ to @.

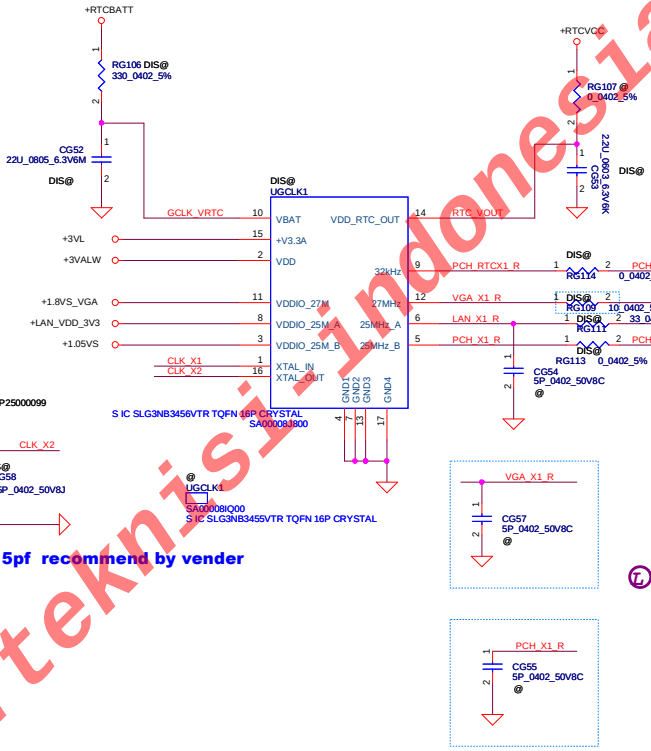


Layout notes
CG47 Close UGCLK1.11
CG48 Close UGCLK1.13
CG49 Close UGCLK1.8
CG50 Close UGCLK1.15
CG41 Close UGCLK1.2

SI phase 20141225
Change YG1 PN to SJ10000FO00



<SI> Change CG59 to 12pf , CG58 to 15pf recommend by vender



20141120
add RG115 RG116 isolated GreenCLKtail
from vendor suggest

Layout notes
Please place RG114, RG109, RG111 and RG113 close to UGCLK1 for Impedance matching.

Change RG109 to 10 ohm recommend by vender

<CPU> YC1 P6
<GPU> Y6 P37
<LAN> YL1 P22
<CPU> YC2 P7

Layout notes
For isolated GreenCLK tail
RG110 close to Y6 (27M for GPU)
RG112 close to YL1 (25M for LAN)
RG115 close to YC1 (32.768k for CPU)
RG116 close to YC2 (24M for CPU)

Layout notes
Place CG57 between UGCLK1 and RG109
Reserve CG55 for vendor Place between UGCLK1 and RG113

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Issued Date	2013/06/10	Deciphered Date	2014/07/01

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Compal Electronics, Inc.

Title: GCLK

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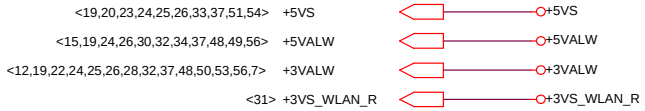
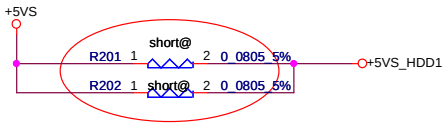
Date: Saturday, January 31, 2015 | Sheet 28 of 61

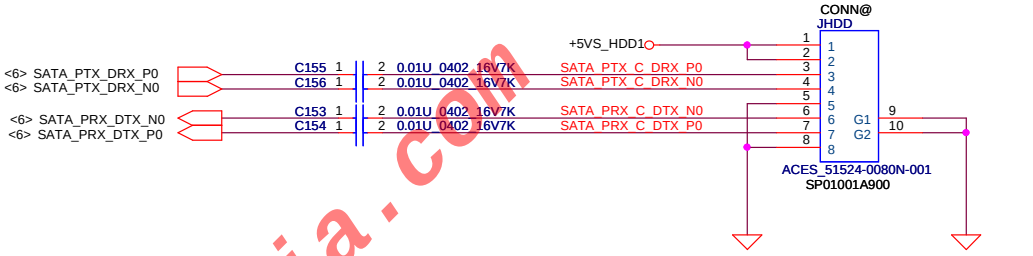
2.5" SATA HDD





HDD power on sub board.

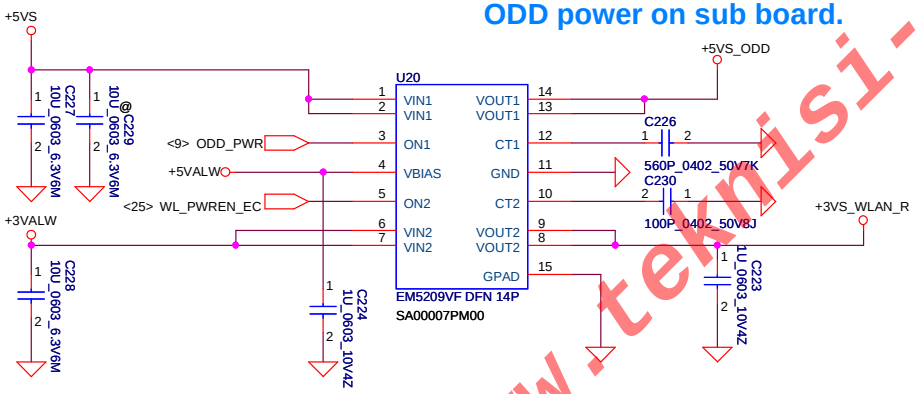
PV : Change R201,R202 to 0-ohm shortpad.
20150125

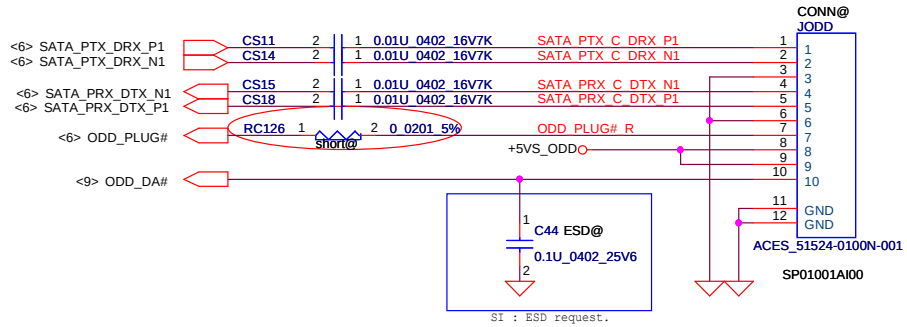


SI : Change HDD pin define.
Follow Cocoa. 12/25

2.5" SATA ODD

ODD power on sub board.





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Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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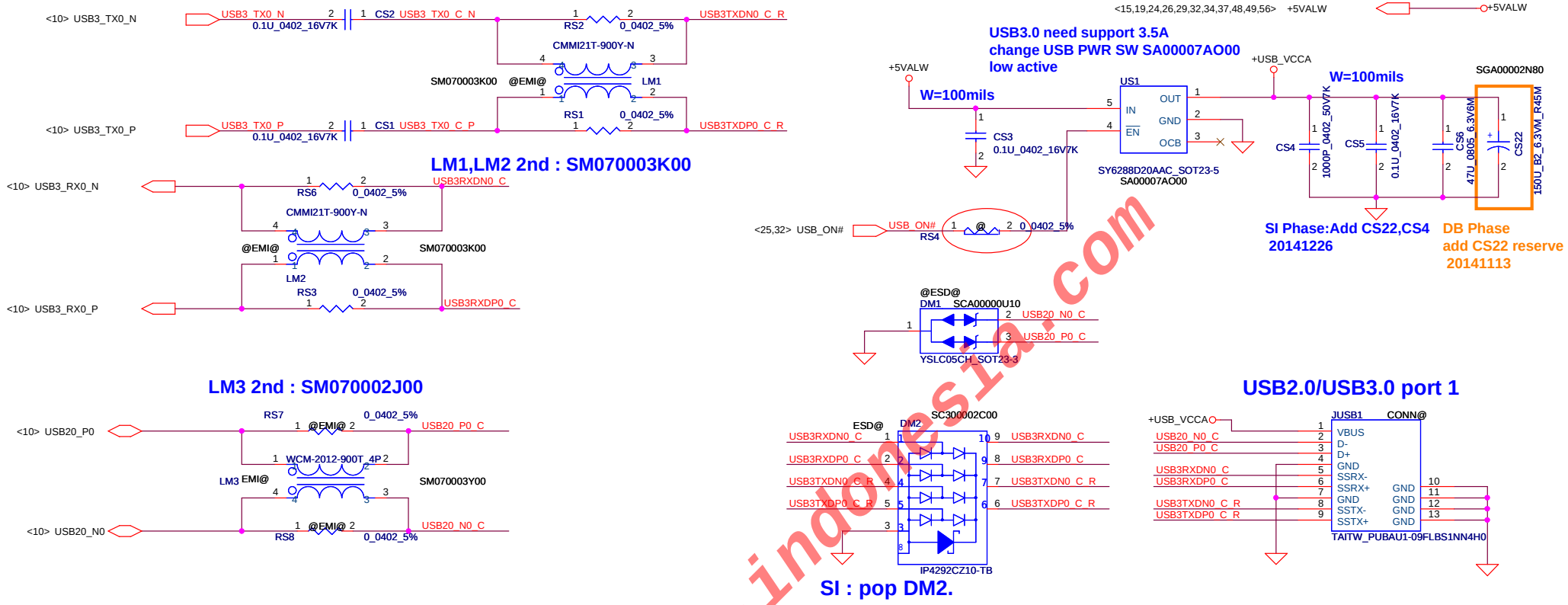
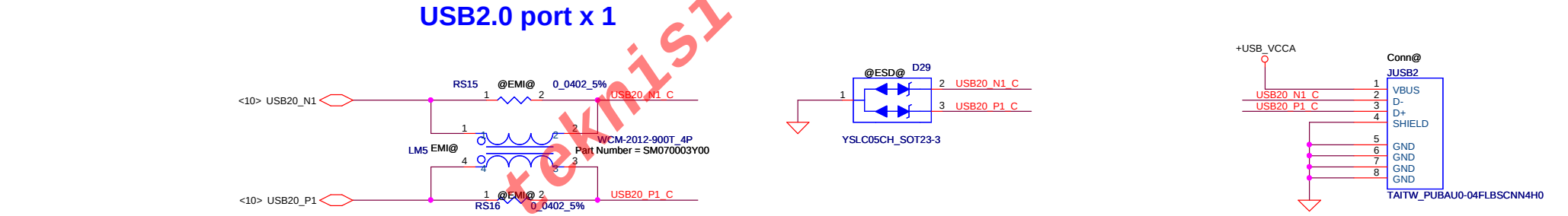
Compal Electronics, Inc.

Title: HDD/ODD Conn

Size: B | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 29 of 61





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Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: USB 3.0/2.0 conn
				Size: B; Document Number: LA-D703P; Rev: 0.1
				Date: Saturday, January 31, 2015; Sheet 30 of 61

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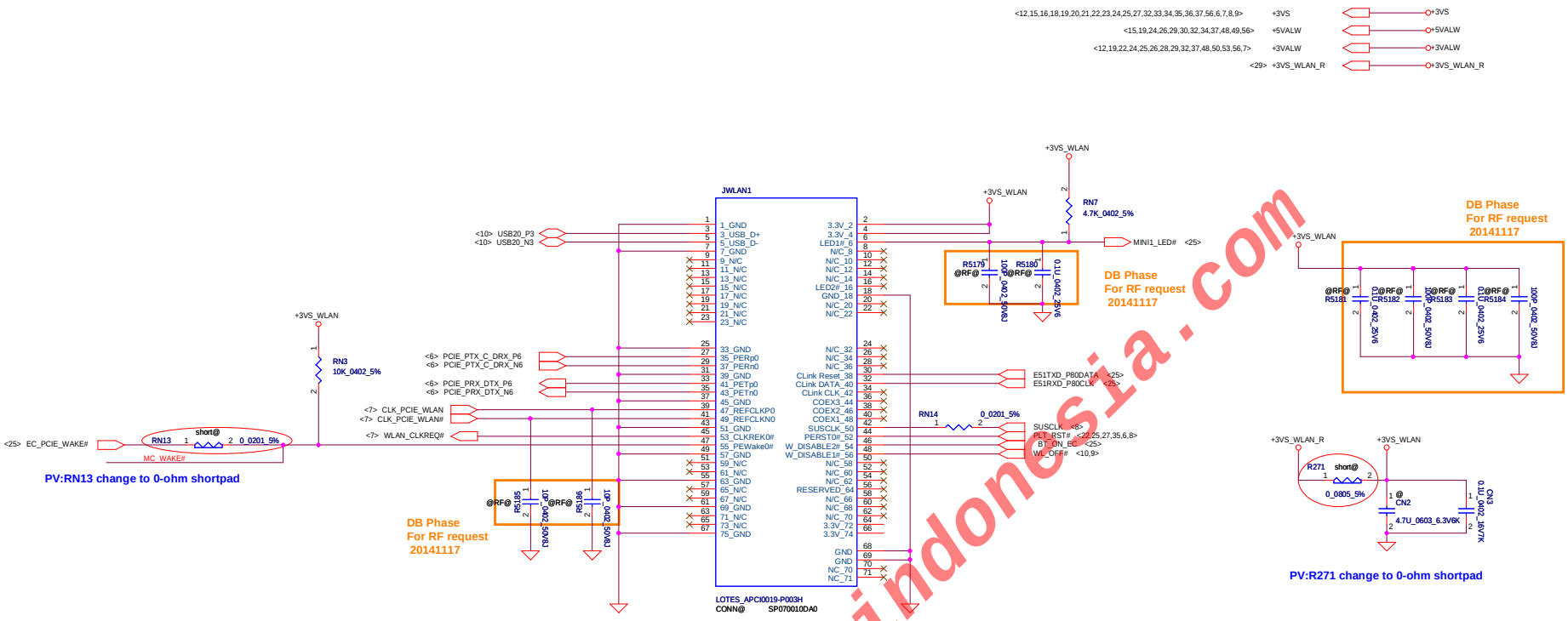
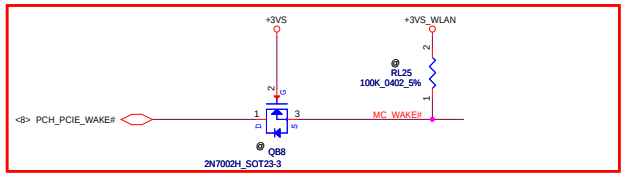


NGFF and WLAN



Unpop QB4 and RL23 for not support OBFF

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Issued Date	2013/02/26	Deciphered Date	2015/07/08

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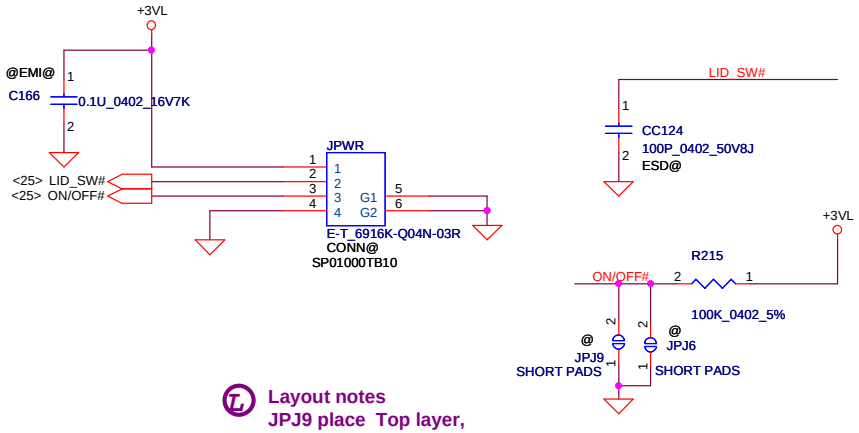
Compal Electronics, Inc.

Title: **WLAN-BT**

Size	Document Number	Rev
	LA-D703P	0.1

Date: Saturday, January 31, 2015 Sheet 31 of 61

Powert Button Connector

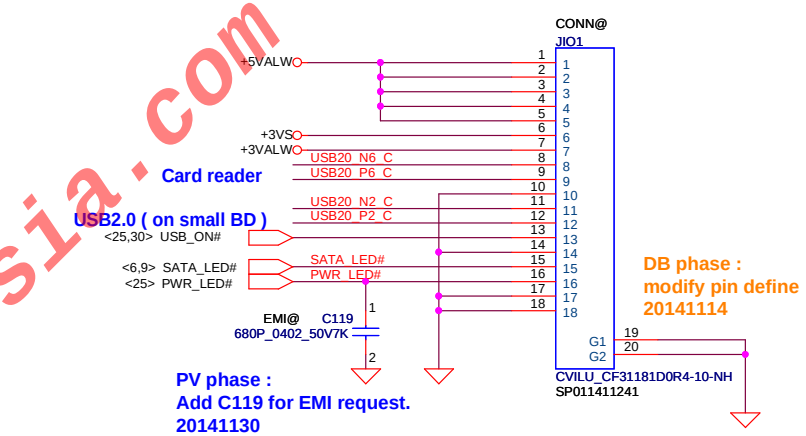


Layout notes
JPJ9 place Top layer,
JPJ6 place Bottom layer

<25,28,46,47,48,6> +3VL
<15,19,24,26,29,30,34,37,48,49,56> +5VALW
<12,15,16,18,19,20,21,22,23,24,25,27,31,33,34,35,36,37,56,6,7,8,9> +3VS
<12,19,22,24,25,26,28,29,37,48,50,53,56,7> +3VALW

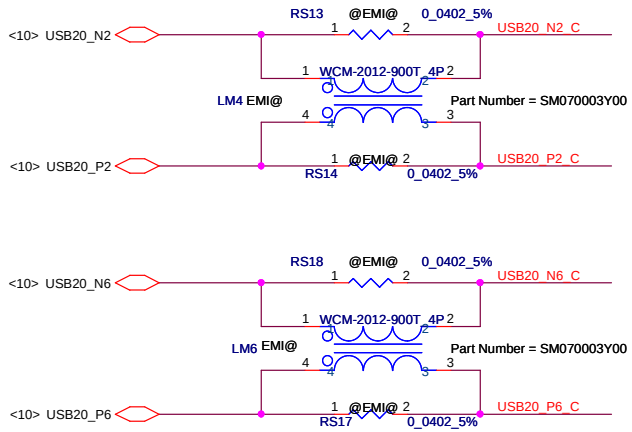
IO BD Connector (USB2.0,Card reader,HDD & PWR LED)

11/26 change CONN.



DB phase :
modify pin define
20141114

PV phase :
Add C119 for EMI request.
20141130



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Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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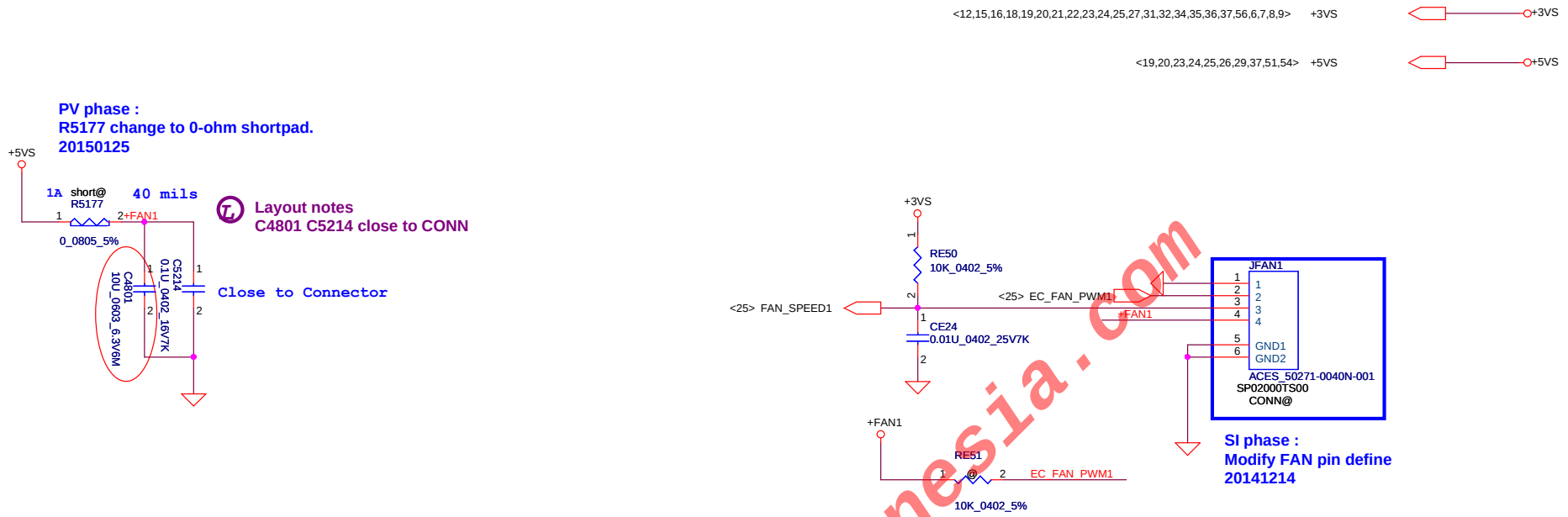
Compal Electronics, Inc.

Title	IO CON	
Size B	Document Number LA-D703P	Rev 0.1
Date: Saturday, January 31, 2015	Sheet 32 of 61	



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Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: FAN
				Size: B; Document Number: LA-D703P; Rev: 0.1
				Date: Saturday, January 31, 2015; Sheet 33 of 61

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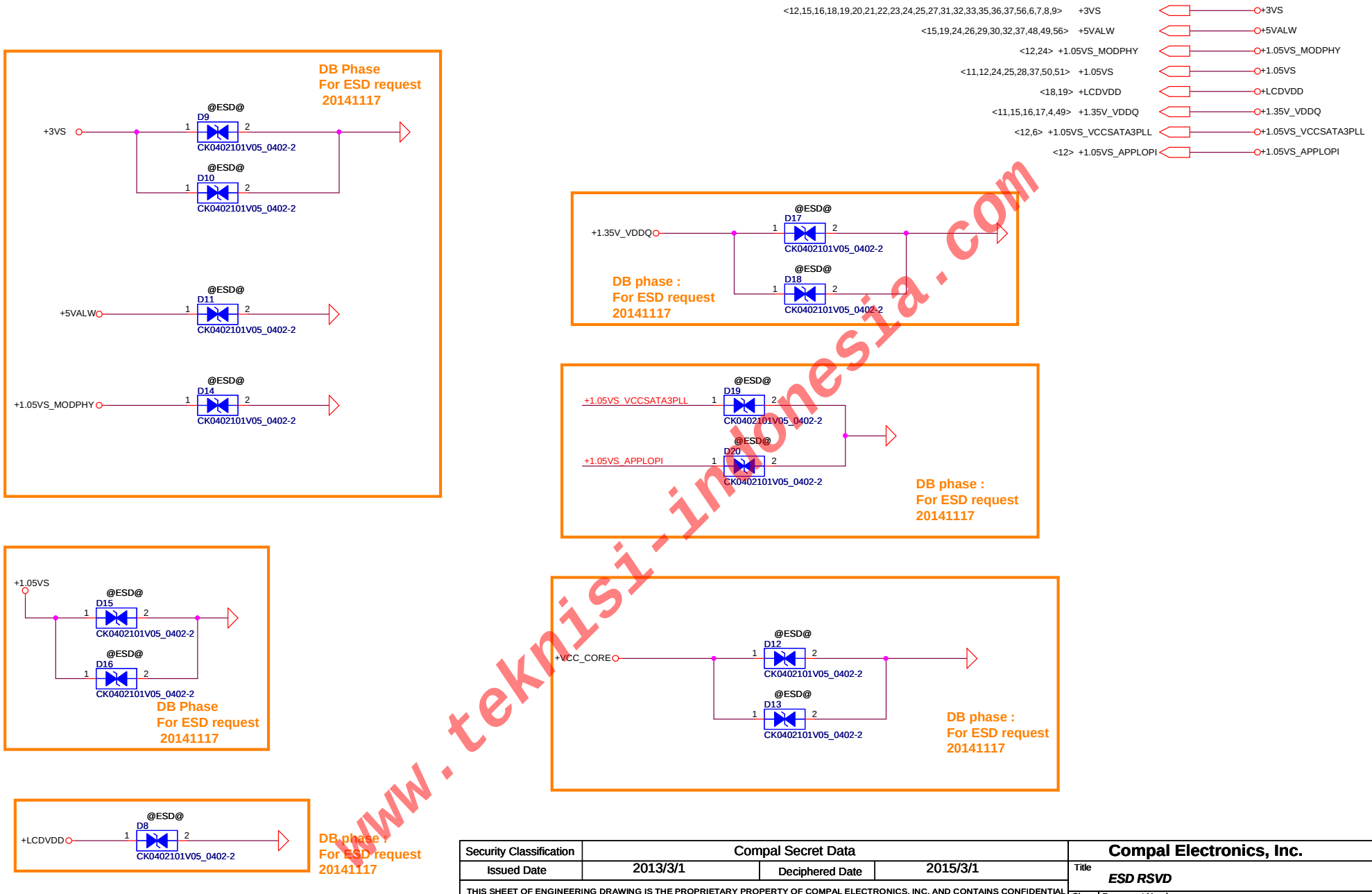

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Security Classification	Compal Secret Data		
Issued Date	2013/3/1	Deciphered Date	2015/3/1

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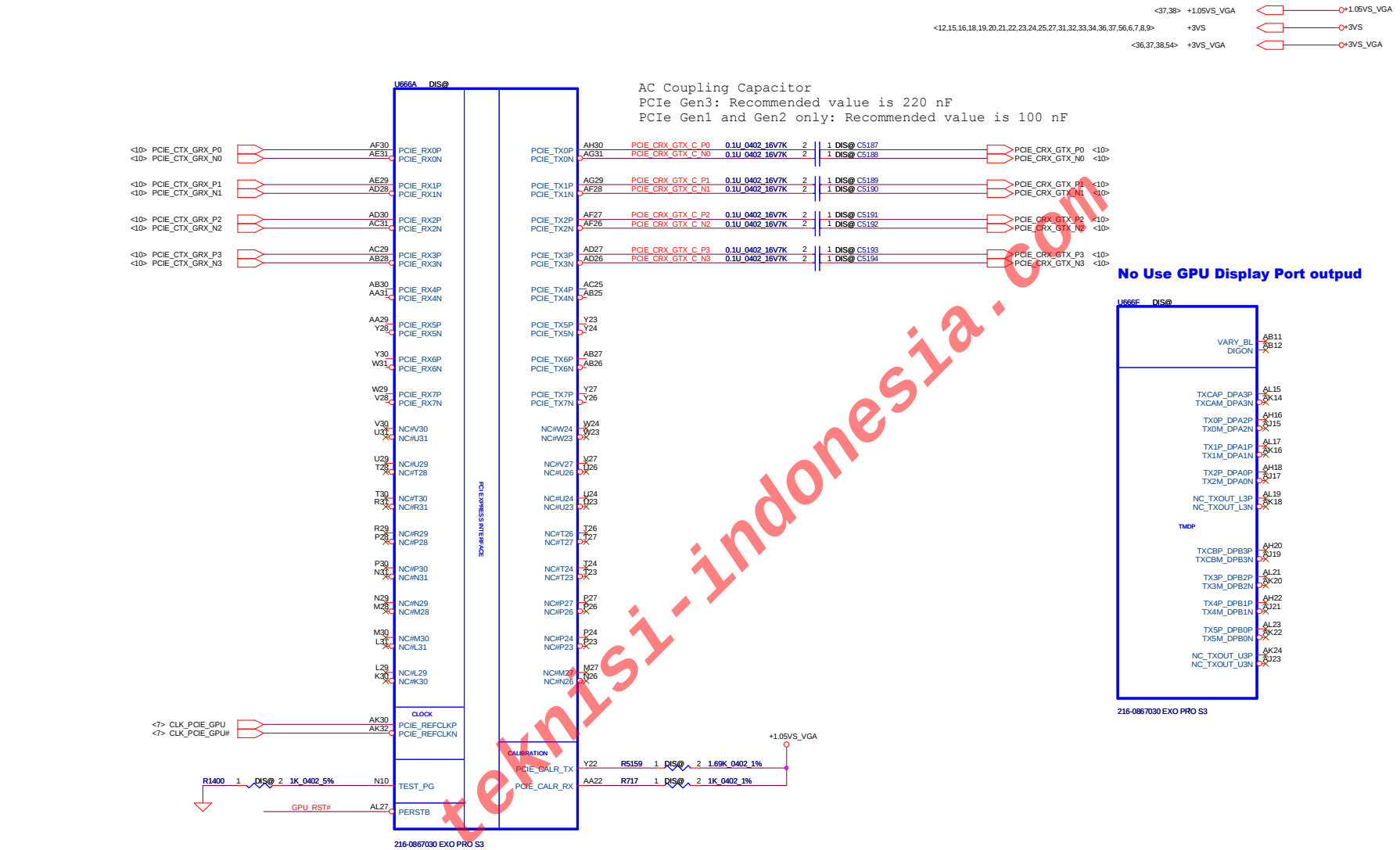
Compal Electronics, Inc.

Title: *ESD RSVD*

Size: | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 34 of 61



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Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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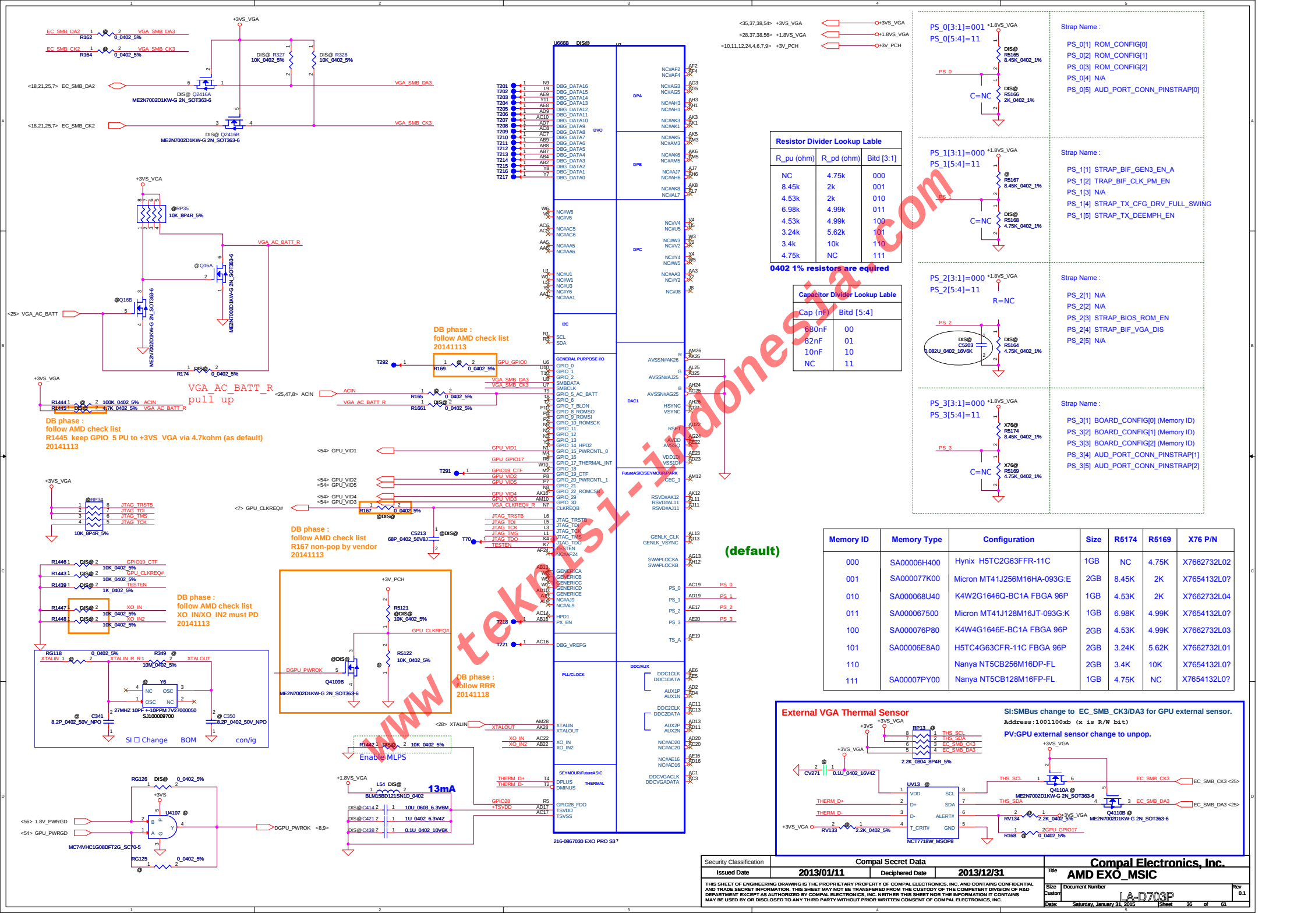
Compal Electronics, Inc.

Title: **AMD EXO_PCIE/DP**

Size: Custom | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 35 of 61



Memory ID	Memory Type	Configuration	Size	R5174	R5169	X76 P/N
000	SA00006H400	Hynix H5TC2G63FFR-11C	1GB	NC	4.75K	X7662732L02
001	SA000077K00	Micron MT41J256M16HA-093G:E	2GB	8.45K	2K	X7654132L0?
010	SA000068U40	K4W2G1646Q-BC1A FBGA 96P	1GB	4.53K	2K	X7662732L04
011	SA000067500	Micron MT41J128M16JT-093G:K	1GB	6.98K	4.99K	X7654132L0?
100	SA000076P80	K4W4G1646E-BC1A FBGA 96P	2GB	4.53K	4.99K	X7662732L03
101	SA00006E8A0	H5TC4G63CFR-11C FBGA 96P	2GB	3.24K	5.62K	X7662732L01
110		Nanya NT5CB256M16DP-FL	2GB	3.4K	10K	X7654132L0?
111	SA00007PY00	Nanya NT5CB128M16FP-FL	1GB	4.75K	NC	X7654132L0?

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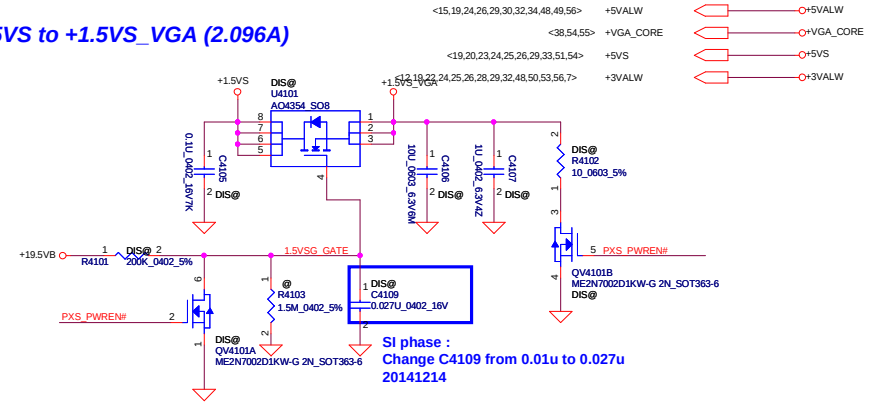
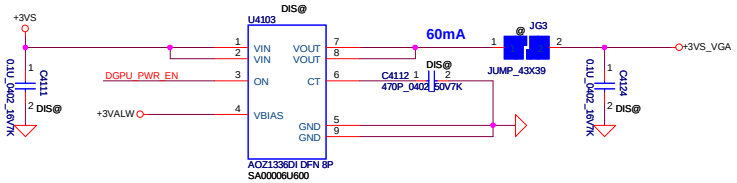
+1.5VS to +1.5VS_VGA (2.096A)



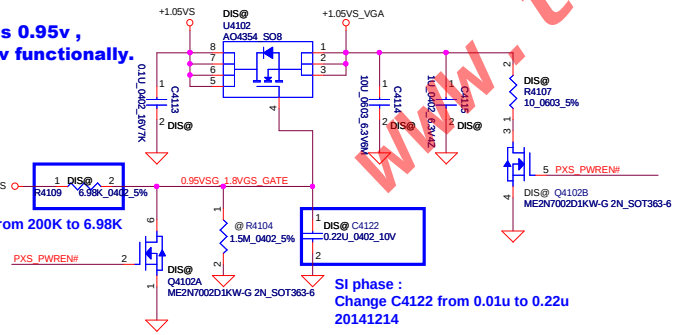
SI phase :
Change C4109 from 0.01u to 0.027u
20141214

+3VS to +3VS_VGA (25mA)



+1.05VS to +1.05VS_VGA (2A)

AMD feedback :
Exo ASIC normally is 0.95v ,
can support to 1.05v functionally.



SI phase :
Change R4109 from 200K to 6.98K
20141214

SI phase :
Change C4122 from 0.01u to 0.22u
20141214

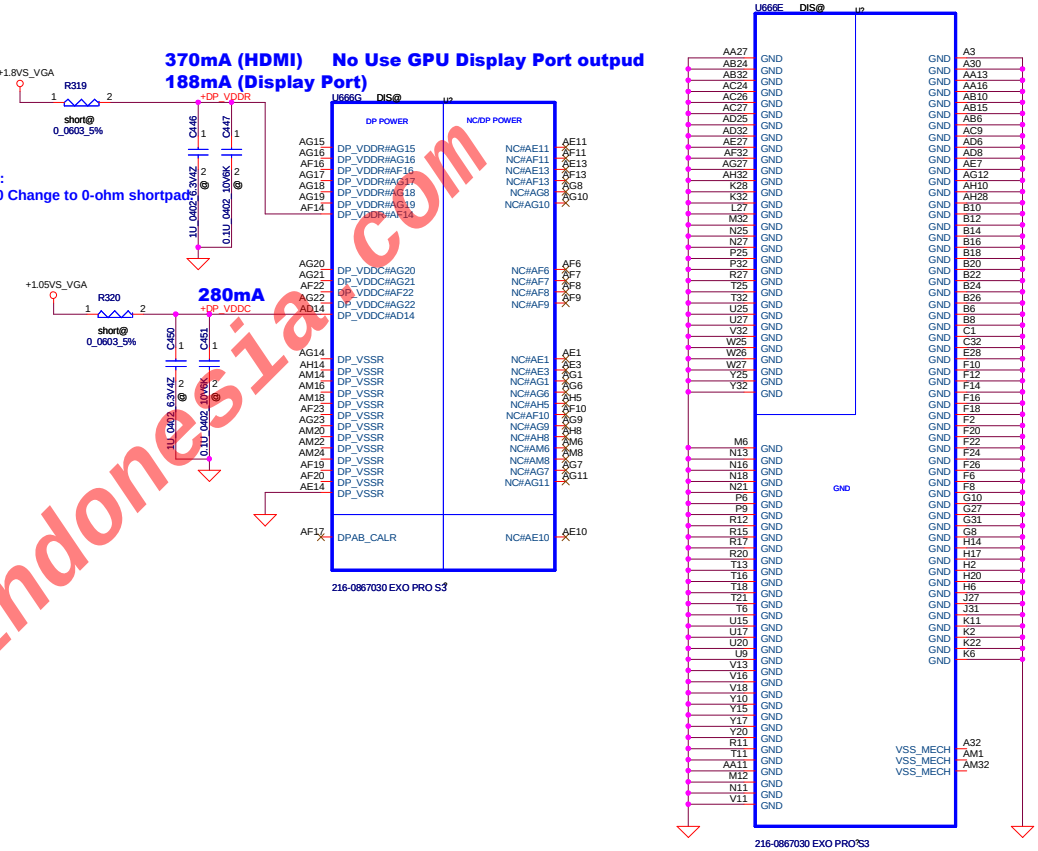
<56> 0.95VSG_1.8VGS_GATE

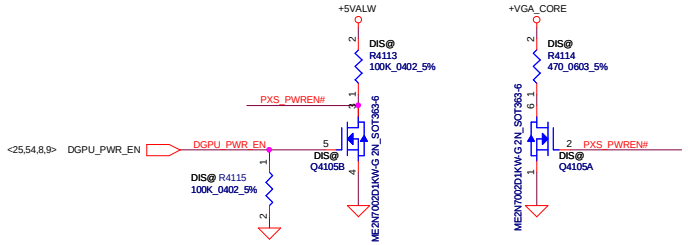
<12,23,53,6> +1.5VS
<38,39,40,41> +1.5VS_VGA
<12,15,16,18,19,20,21,22,23,24,25,27,31,32,33,34,35,36,56,6,7,8,9> +3VS
<35,36,38,54> +3VS_VGA
<11,12,24,25,28,34,50,51> +1.05VS
<35,38> +1.05VS_VGA
<19,47,48,49,51,53,54> +19.5VB

370mA (HDMI) **No Use GPU Display Port outpud**
188mA (Display Port)

PV phase :
R319,R320 Change to 0-ohm shortpad
20150125

280mA





Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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Compal Electronics, Inc.

Title: **AMD EXO_Power/GND**

Size: Custom | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 37 of 61

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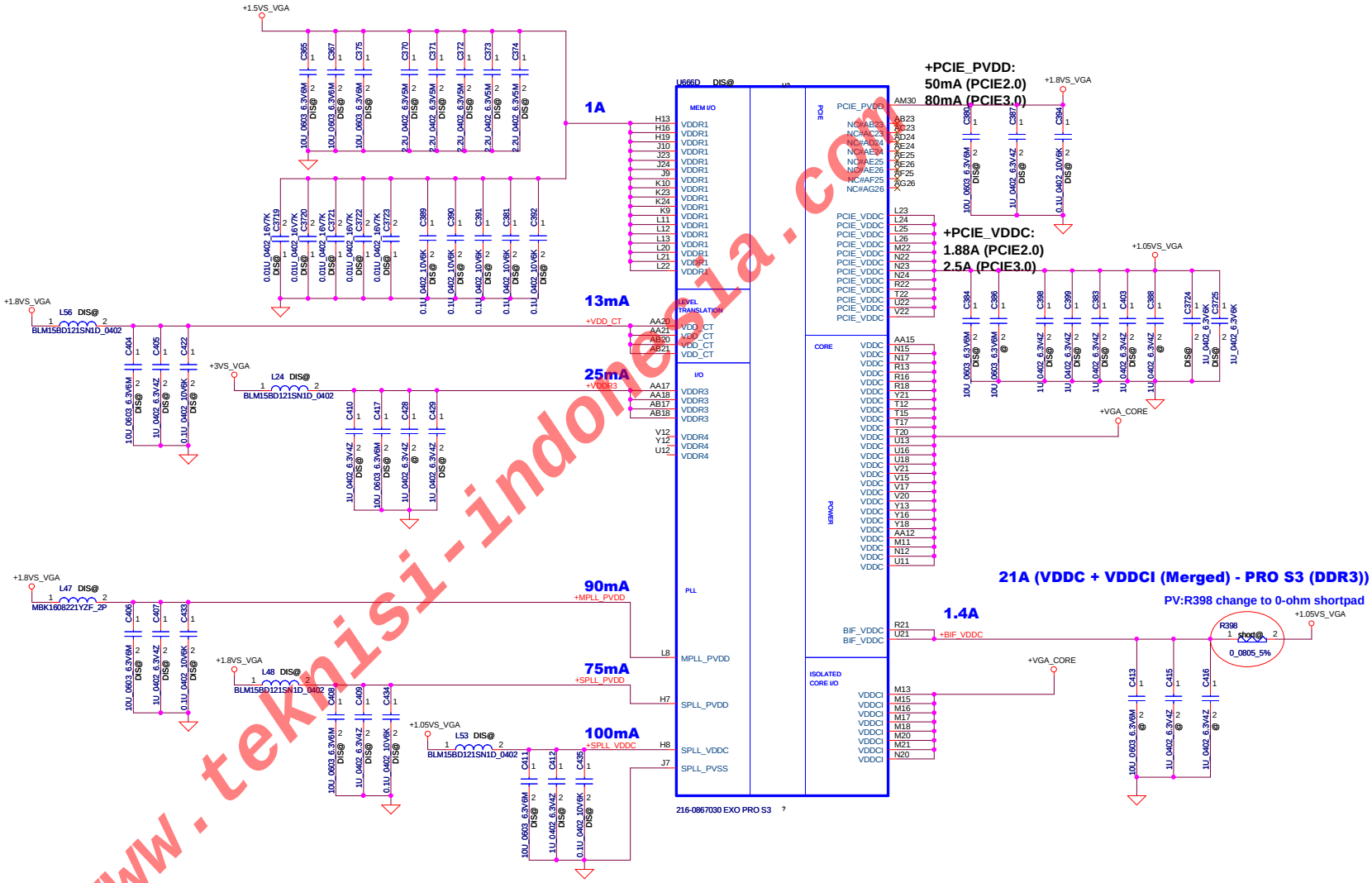
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+0.95VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



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Compal Electronics, Inc.

Title: AMD EXO_Power

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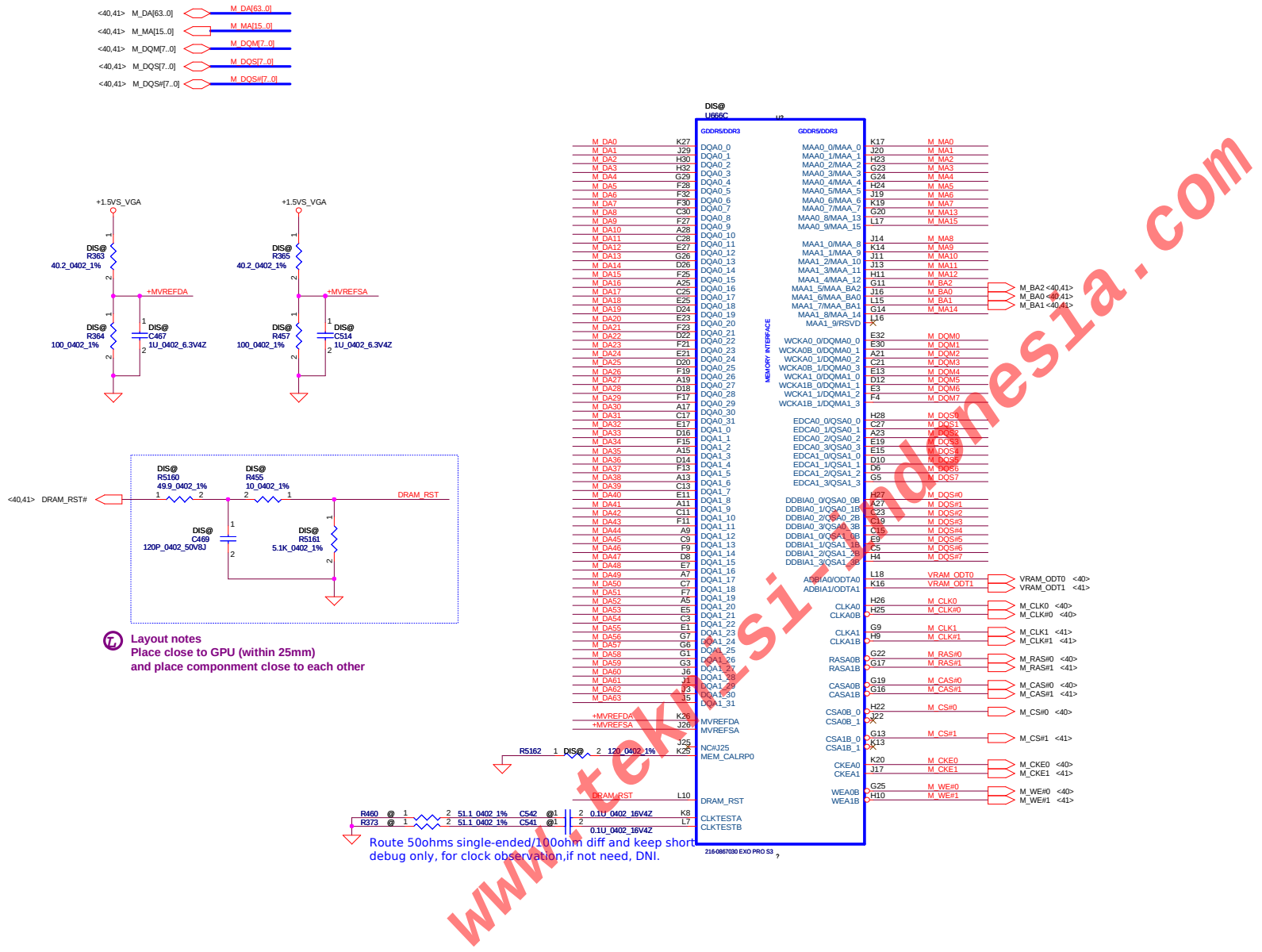

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Compal Electronics, Inc.

Title: **AMD EXO_MEM**

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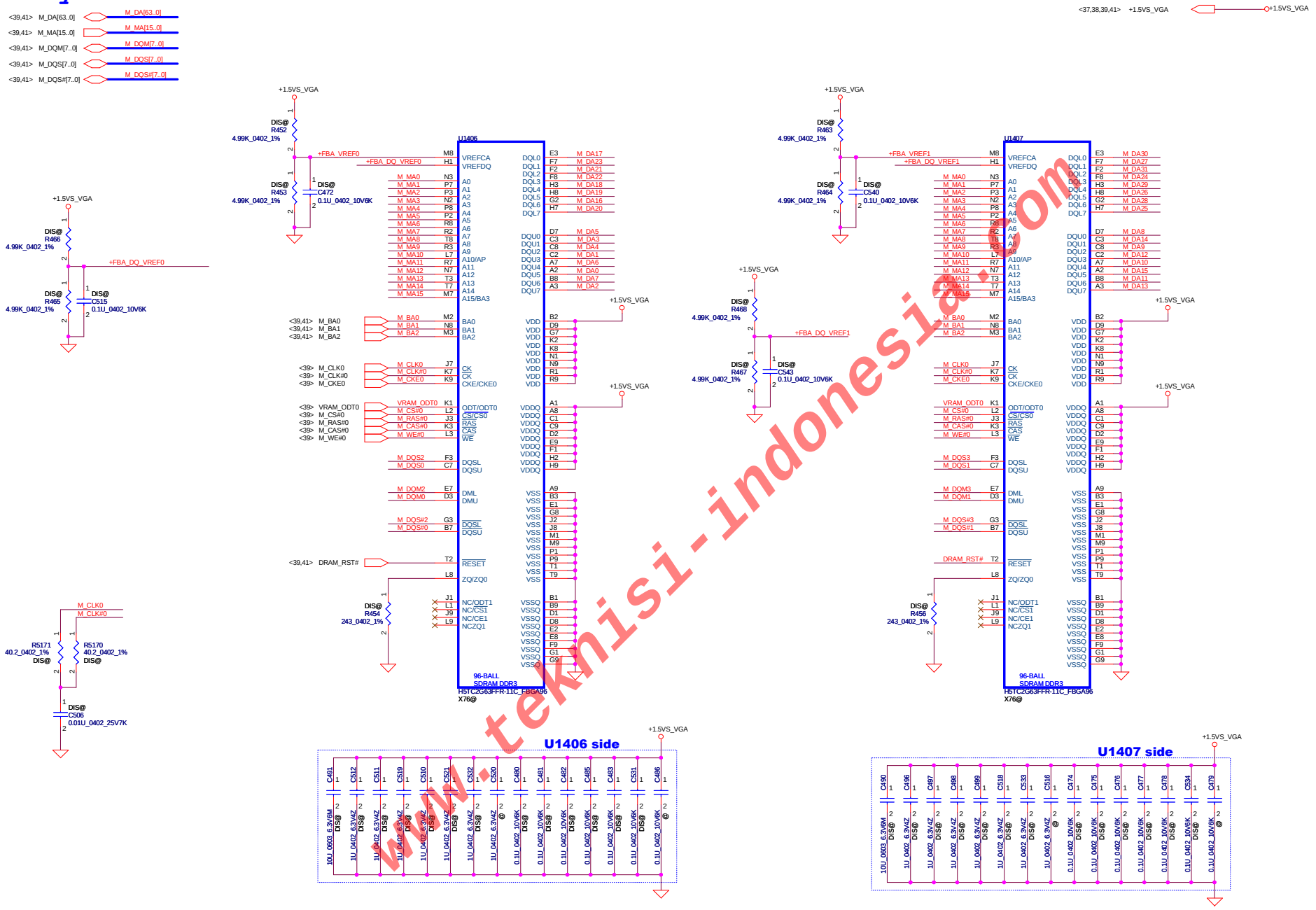
Memory Partition A - Lower 32 bits



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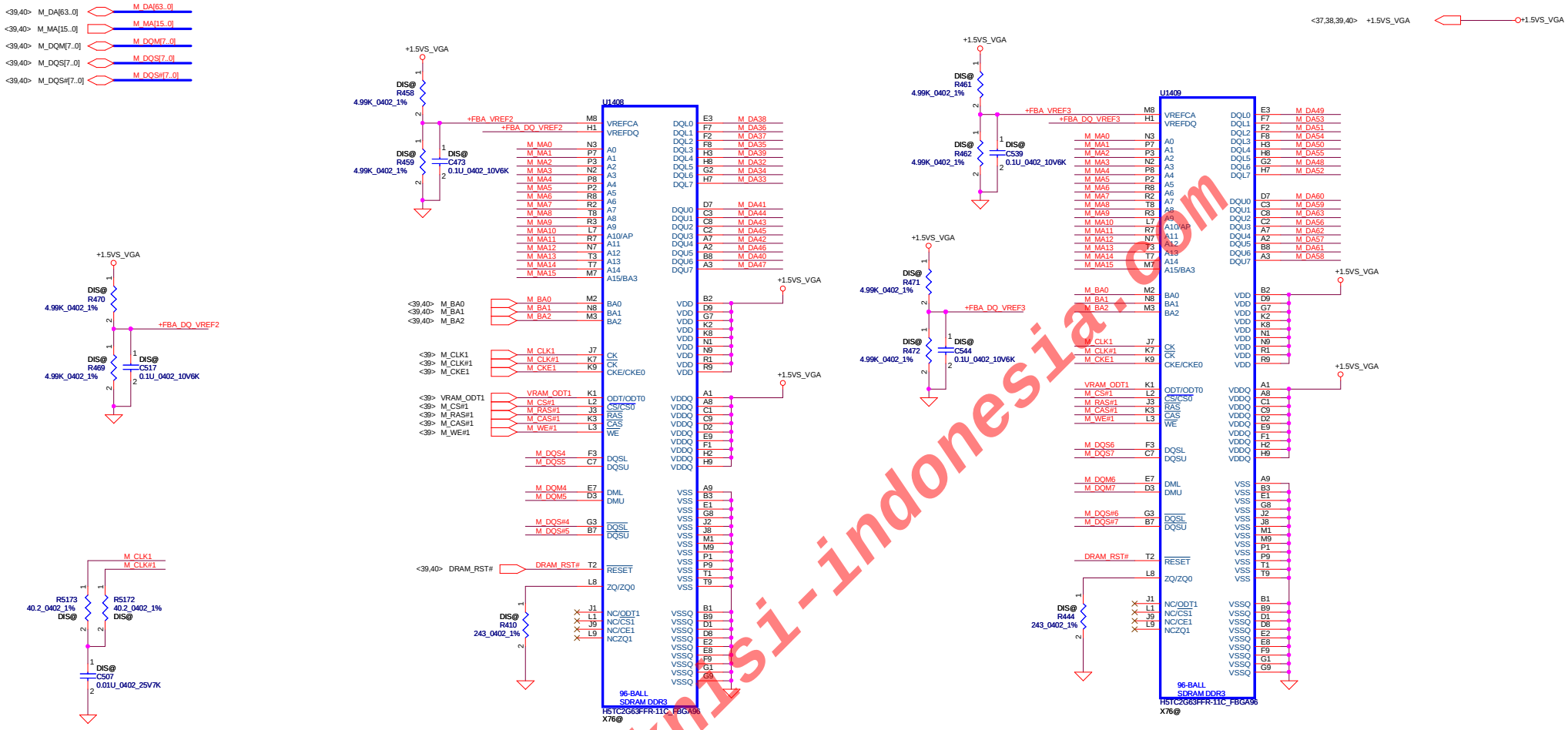
Compal Electronics, Inc.

Title: **AMD EXO_VRAM A Lower**

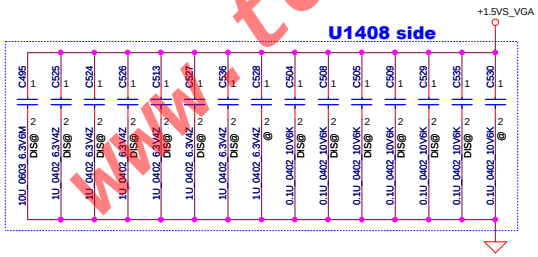
Size: Custom | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 40 of 61

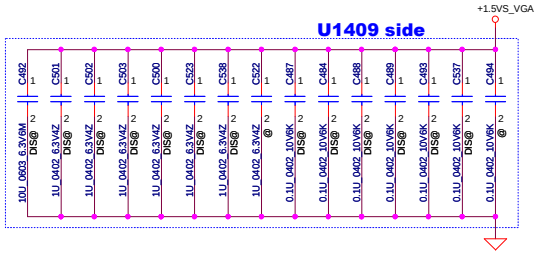
Memory Partition A - Upper 32 bits



U1408 side



U1409 side



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Compal Electronics, Inc.

Title: AMD EXO_VRAM A Upper

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DB build CPU type

UCPU1
2.4G@
i7-5500U BDW
SA000089A00

UCPU1
2.0G@
i3-5005U BDW
SA000083E50

UCPU1
1.7G@
i3 4005U
SA000072Q80

ZZZ004
HY1@
1G Hynix
X7662732L02

ZZZ004
HY2@
2G Hynix
X7662732L01

ZZZ
DAX
DA6001DO000

ZZZ004
SAM2@
2G SAMSUNG
X7662732L03

ZZZ004
SAM1@
1G SAMSUNG
X7662732L04

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Compal Electronics, Inc.

Title: ***BOM control***

Size: | Document Number: LA-D703P | Rev: 0.1

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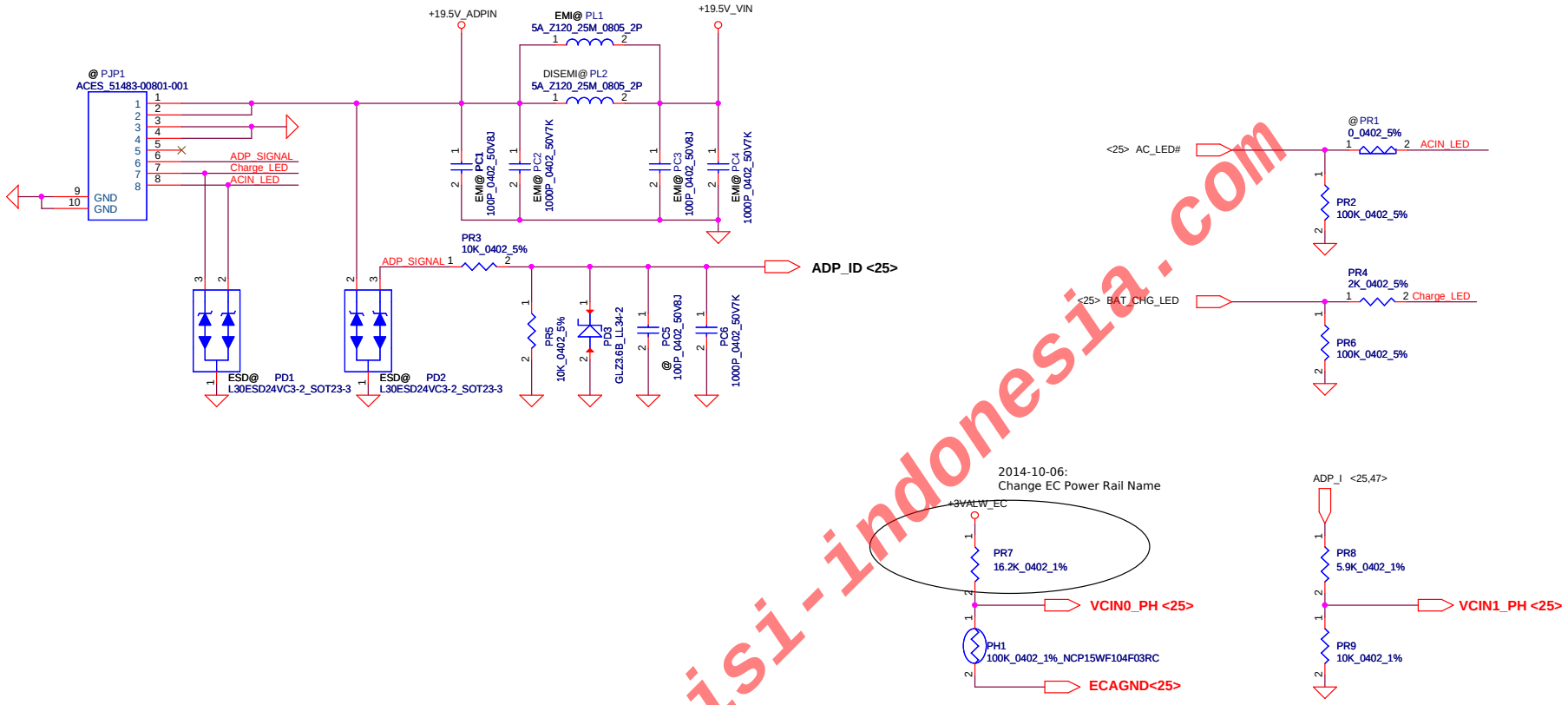

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Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2017/10/09

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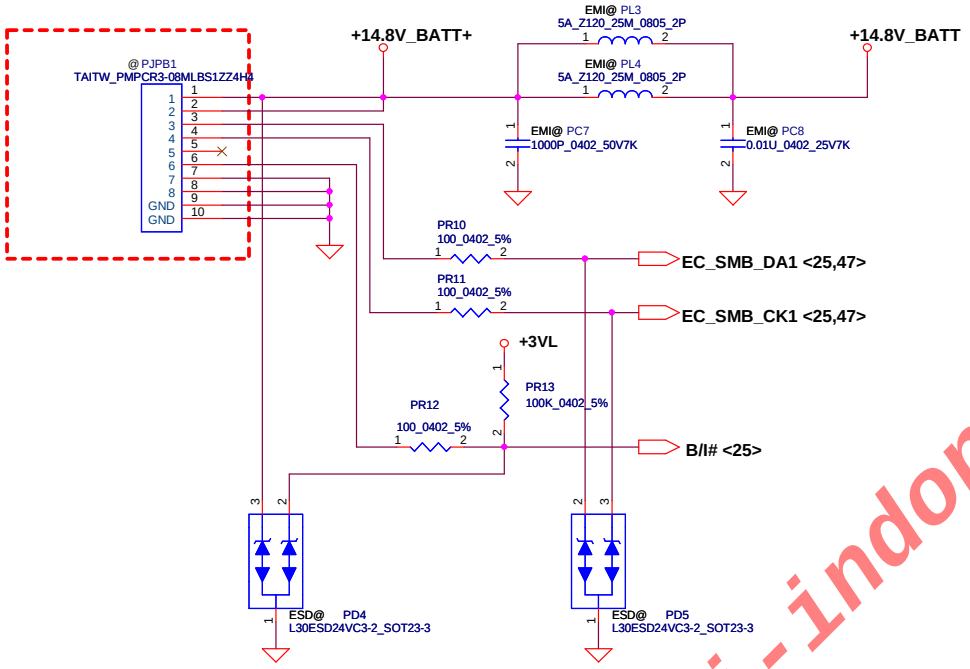
Compal Electronics, Inc.

Title: ***DC Conn***

Size | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 45 of 60



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Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2017/10/09

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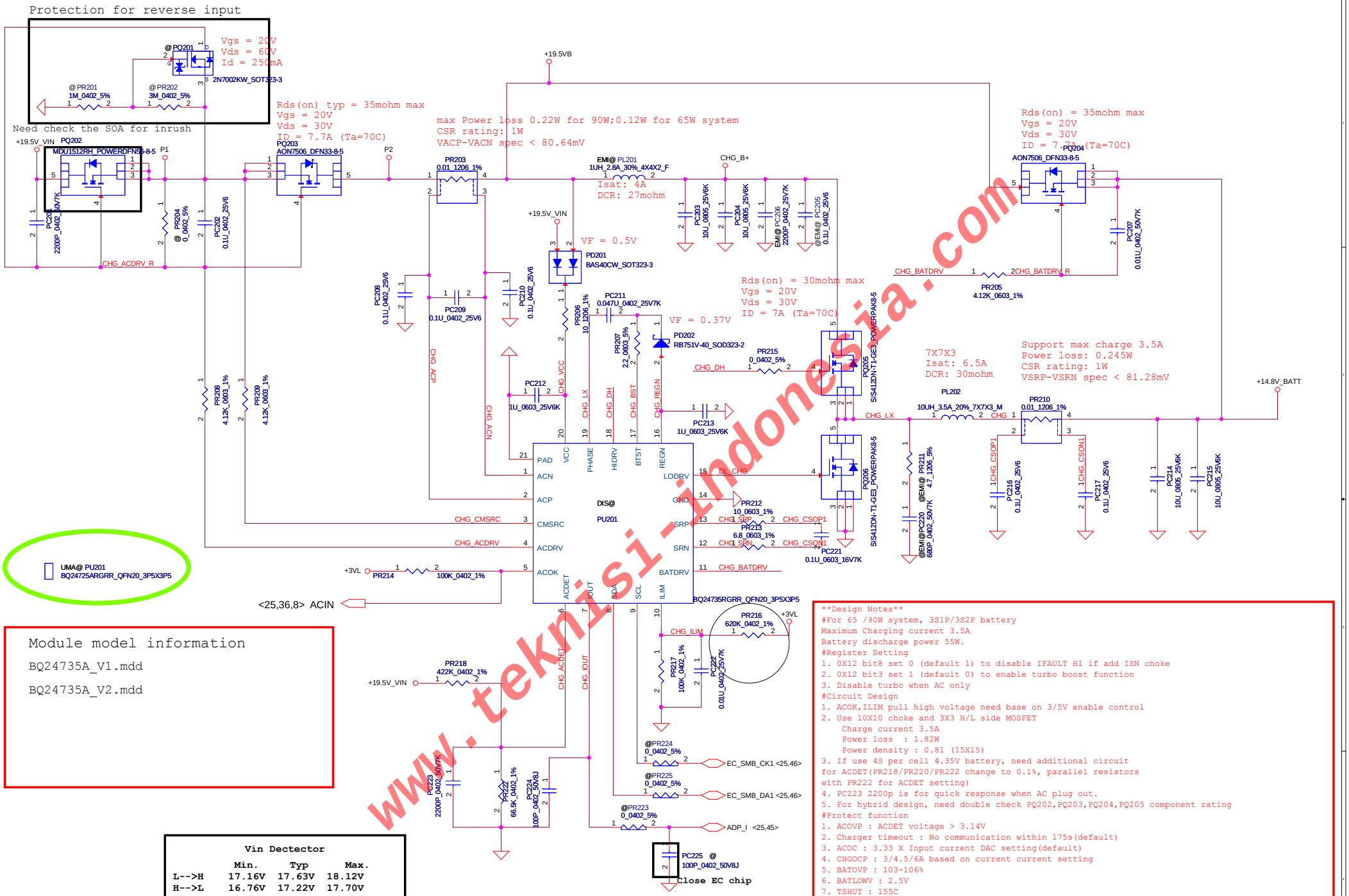
Compal Electronics, Inc.

Title: ***BATT Conn***

Size | Document Number: LA-D703P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 46 of 60



Module model information

BQ24735A_V1.mdd

BQ24735A_V2.mdd

Vin Dectector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+620)/20/0.01
= 2.29 A

```
**Design Notes**
#For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Battery discharge power 55W.
#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
2. 0X12 bit3 set 1 (default 0) to enable turbo boost function
3. Disable turbo when AC only
#Circuit Design
1. ACOK,ILIM pull high voltage need base on 3/5V enable control
2. Use 10X10 choke and 3X3 H/L side MOSFET
    Charge current 3.5A
    Power loss  : 1.82W
    Power density : 0.81 (15X15)
3. If use 4S per cell 4.35V battery, need additional circuit
for ACDET(PR218/PR220/PR222 change to 0.1%, parallel resistors
with PR222 for ACDET setting)
4. PC223 2200p is for quick response when AC plug out.
5. For hybrid design, need double check PQ202,PQ203,PQ204,PQ205 component rating
#Protect function
1. ACOVP : ACDET voltage > 3.14V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVP : 103~106%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 110mV (default)
```

Security Classification	Compal Secret Data		
Issued Date	2014/07/02	Deciphered Date	2012/07/02

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Compal Electronics, Inc.

Title: **PWR-CHARGER**

Size | Document Number: *Common Circuit* | Rev 0.1

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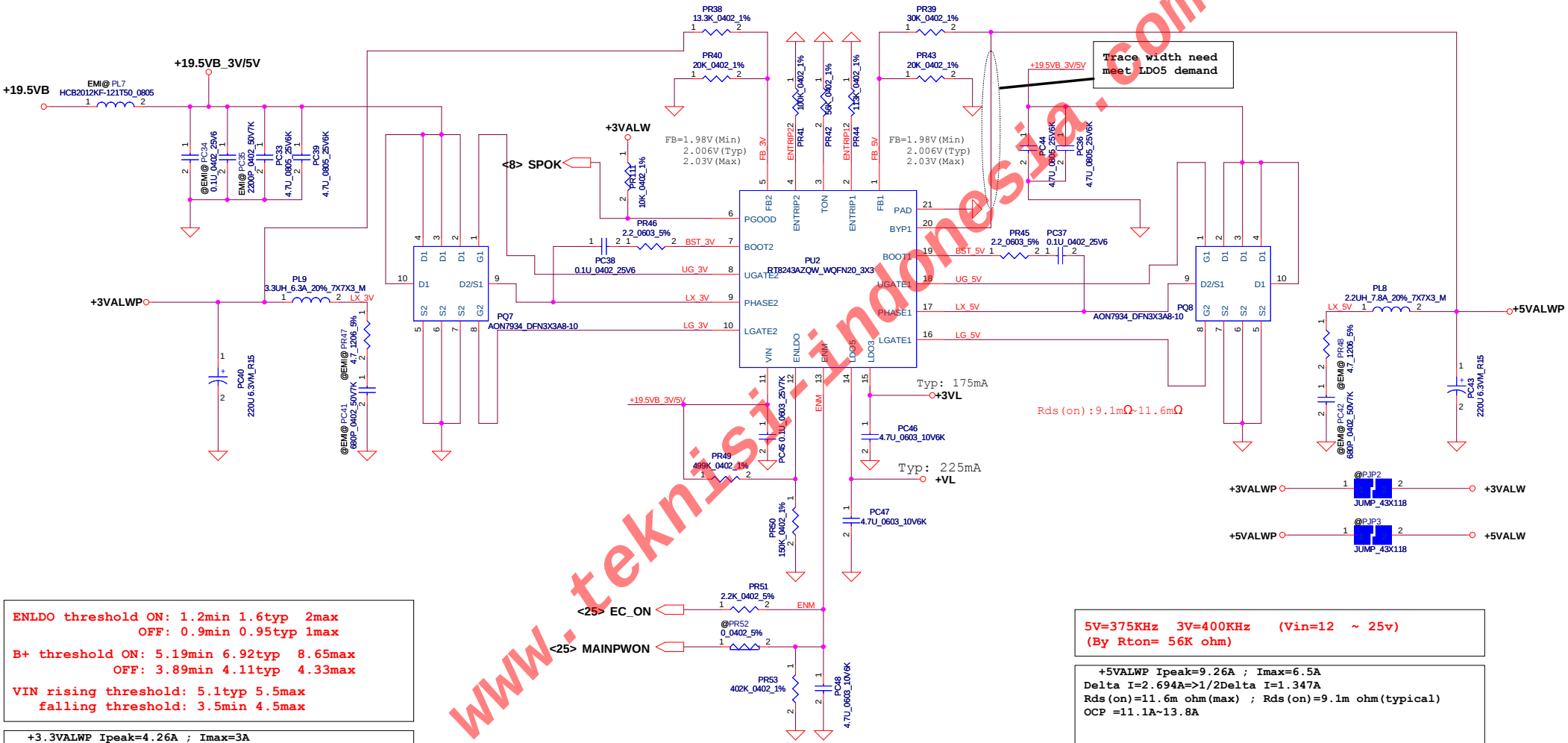
Module model information

RT8243A_V1.mdd

ENTRIPx adjustment range: 0.5V~3V,
floating or over 4.5V will shutdown channel.

ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LDO5	LDO3	+5VALW	+3VALW
Low	Low	X	X	Off	Off	Off	Off
">1.6V" =>High	Low	X	X	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	Off	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	On	On	On	Off	On
">1.6V" =>High	">2.3V" =>High	On	On	On	On	On	On
">1.6V" =>High	">2.3V" =>High	On	Off	On	On	On	Off



ENLDO threshold ON: 1.2min 1.6typ 2max
OFF: 0.9min 0.95typ 1max

B+ threshold ON: 5.19min 6.92typ 8.65max
OFF: 3.89min 4.11typ 4.33max

VIN rising threshold: 5.1typ 5.5max
falling threshold: 3.5min 4.5max

+3.3VALWP Ipeak=4.26A ; Imax=3A
Delta I=1.583A=>1/2Delta I=0.7915A
Rds(on)=11.6m ohm(max) ; Rds(on)=9.1m ohm(typical)
OCP = 9.41A~11.8A

TDC:4.31A Fsw:375KHz
H-MOS PD:0.3736W ΔT:12℃℃
L-MOS PD:0.2713W ΔT:7.9℃℃
Choke PD:1.5158W ΔT:24℃℃
OVP margin for Vos:8% @ 330uF cap, 6% @ 220uF

5V=375KHz 3V=400KHz (Vin=12 ~ 25v)
(By Rton= 56K ohm)

+5VALWP Ipeak=9.26A ; Imax=6.5A
Delta I=2.694A=>1/2Delta I=1.347A
Rds(on)=11.6m ohm(max) ; Rds(on)=9.1m ohm(typical)
OCP =11.1A~13.8A

TDC:4.9A Fsw:321KHz
H-MOS PD:0.4173W ΔT:13.4℃℃
L-MOS PD:0.3442W ΔT:10℃℃
Choke PD:1.9613W ΔT:30℃℃
OVP margin for Vos:9% @ 330uF cap, 8% @ 220uF

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Compal Electronics, Inc.

Title: 3VALW/5VALW

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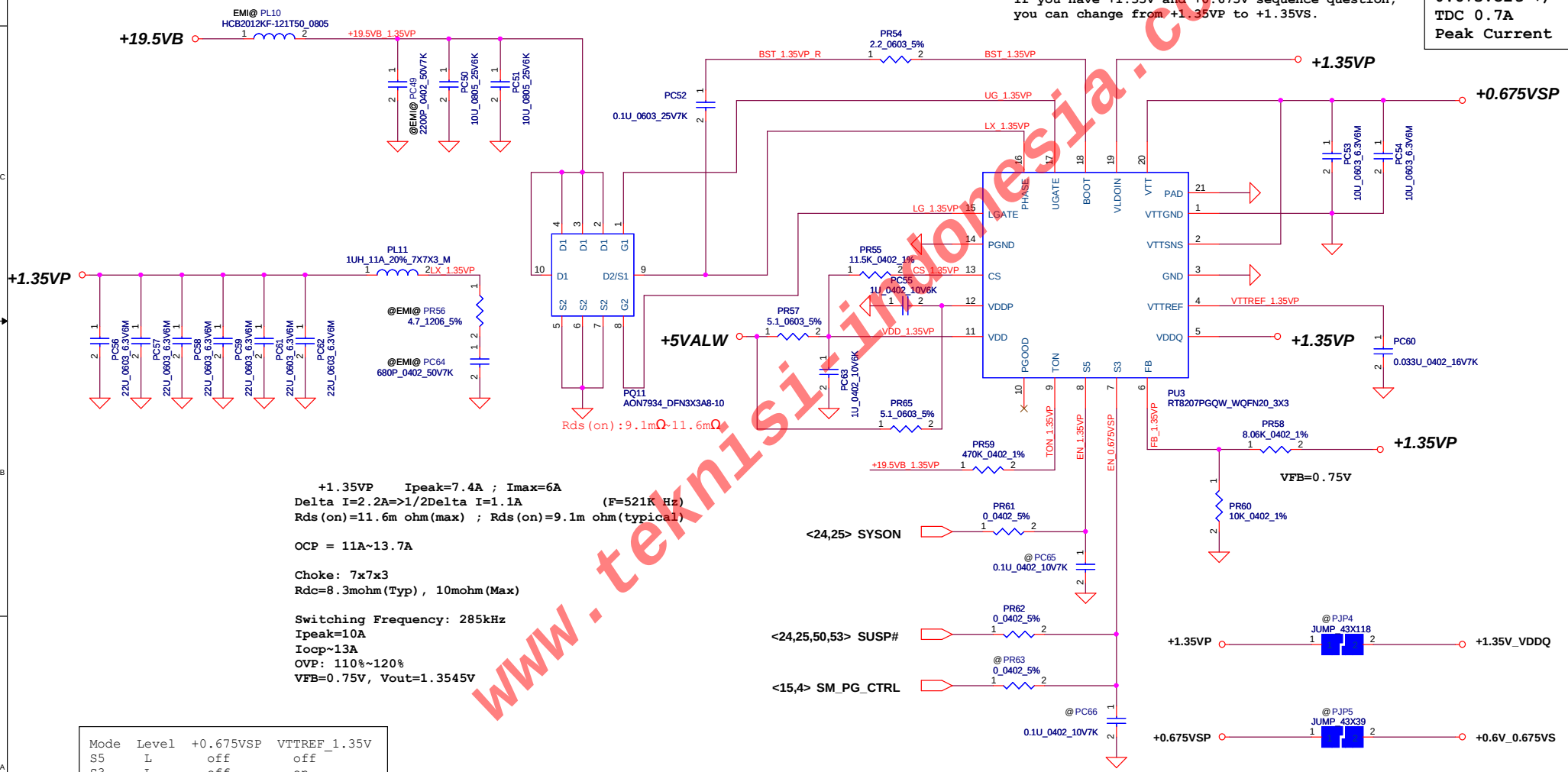
Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



+1.35VP Ipeak=7.4A ; Imax=6A
Delta I=2.2A=>1/2Delta I=1.1A (F=521K Hz)
Rds(on)=11.6m ohm(max) ; Rds(on)=9.1m ohm(typical)

OCP = 11A~13.7A

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
VFB=0.75V, Vout=1.3545V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

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Title: LA-D703P

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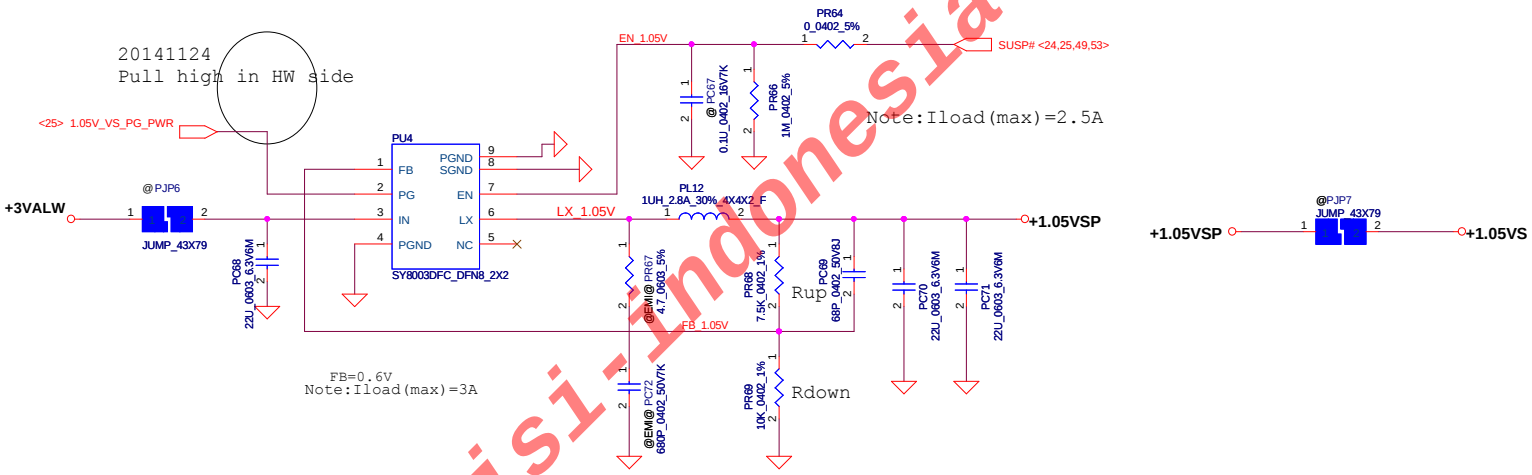
Module model information

SY8003_V2.mdd



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

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Title: **SY8003**

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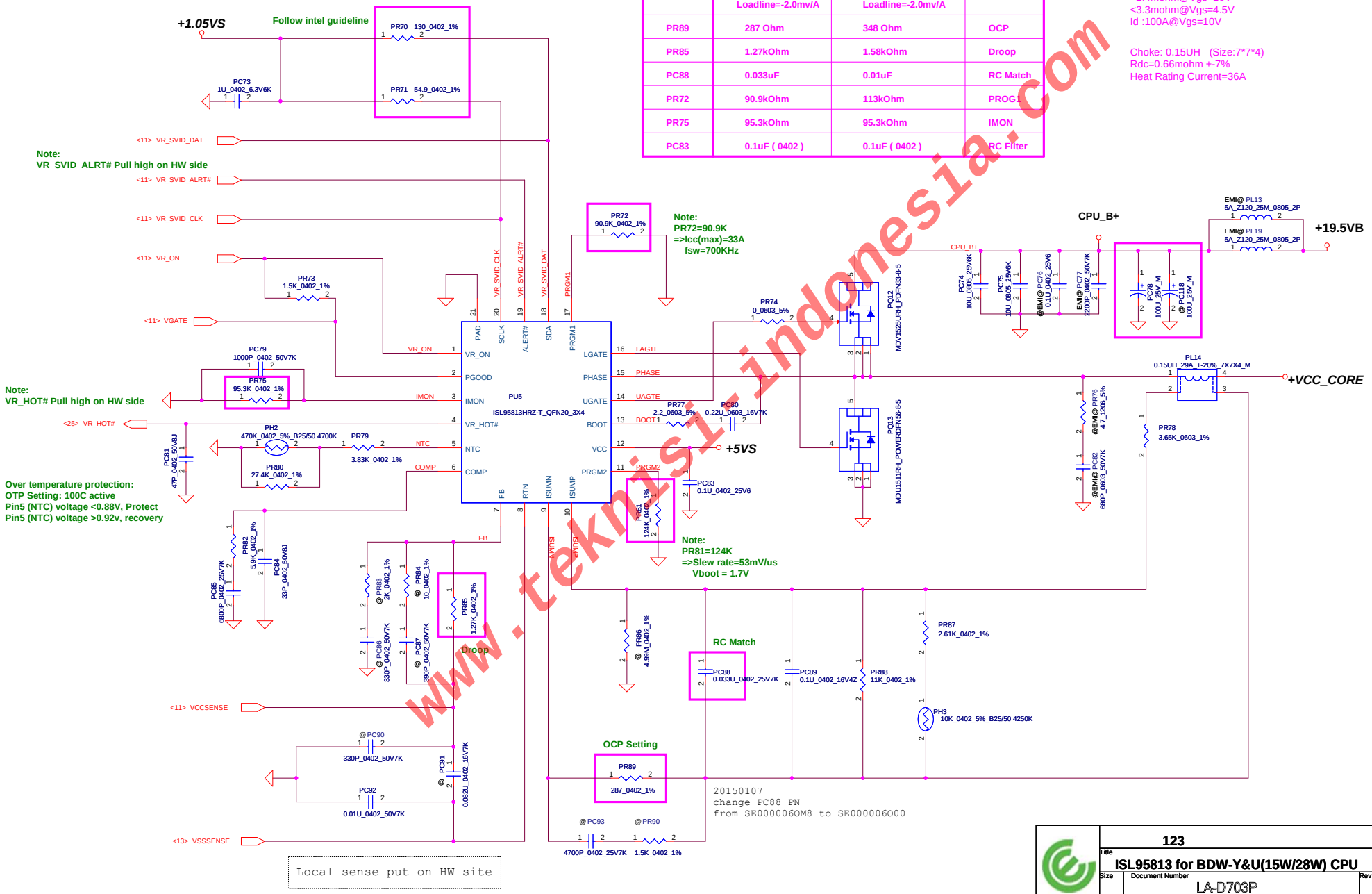
Module model information:
ISL95813_V1A for IC module
ISL95813_V1B for SW module

Base on BDW PDDG Rev_0_73			
Location	15W	28W	Note
	TDC 14A	TDC 19A	
	MAX 32A	MAX 40A	
	OCP 39A	OCP 48A	
	Loadline=-2.0mv/A	Loadline=-2.0mv/A	
PR89	287 Ohm	348 Ohm	OCP
PR85	1.27kOhm	1.58kOhm	Droop
PC88	0.033uF	0.01uF	RC Match
PR72	90.9kOhm	113kOhm	PROG1
PR75	95.3kOhm	95.3kOhm	IMON
PC83	0.1uF (0402)	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.15UH (Size:7*7*4)
Rdc=0.66mohm +-7%
Heat Rating Current=36A



20150107
change PC88 PN
from SE000006OM8 to SE000006000

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123		
Title: ISL95813 for BDW-Y&U(15W/28W) CPU		
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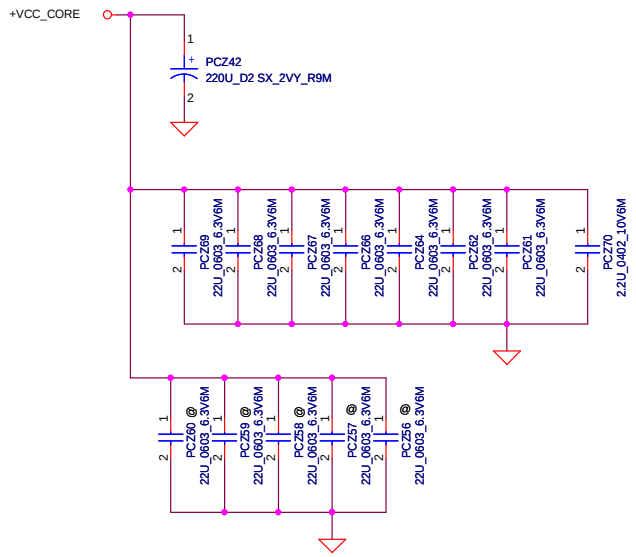

BDW-U 15W
220uF × 1
22uF × 7
2.2uF × 1

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Issued Date	2013/09/09	Deciphered Date	2016/09/30

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Compal Electronics, Inc.

Title: ***PROCESSOR DECOUPLING***

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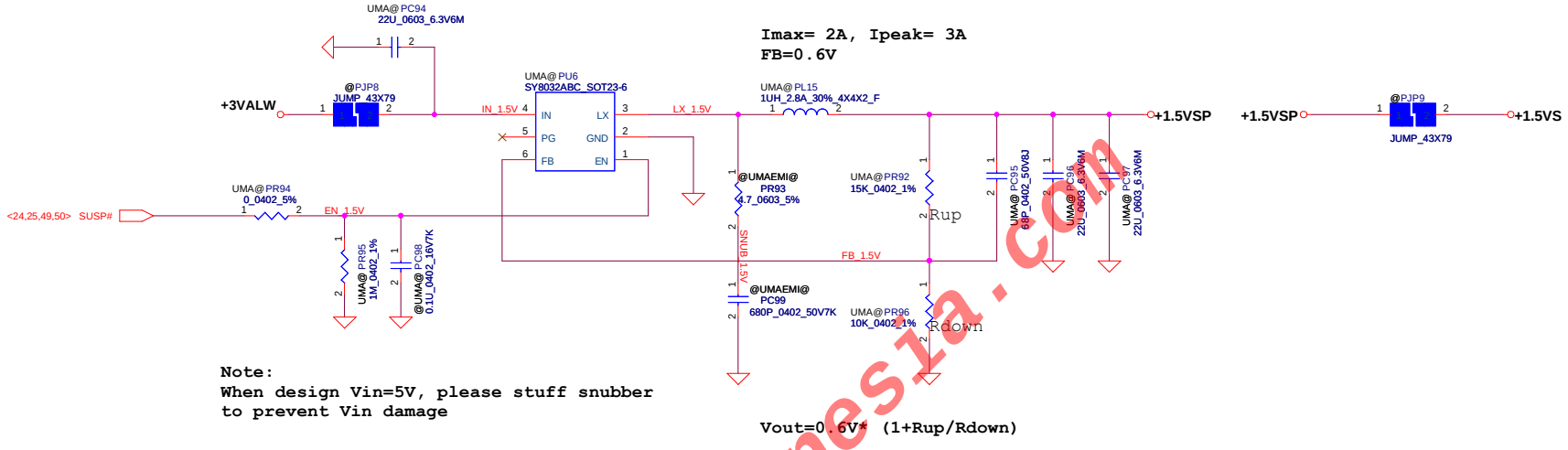
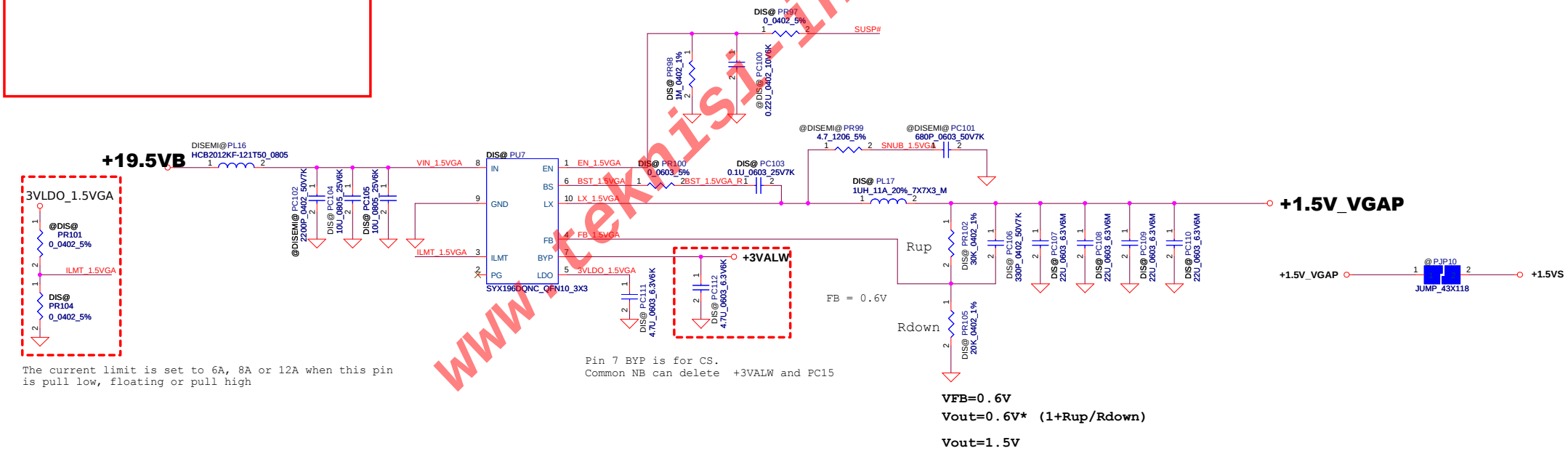


Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

Module model information

SYX196D_V3.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



The current limit is set to 6A, 8A or 12A when this pin
is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)

Vout=1.5V

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GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	0	1.150V
1	0	0	0	0	1.100V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V

Vboot(merge)

	AMD MARS series			LP: DDR3 Pro/XT/XTX: GDDR5	AMD SUN series		UL: DDR3 Pro/XT/XTX: GDDR5	Description
GPU	MARS XTX	MARS XT	MARS PRO	MARS LP	SUN UL	SUN PRO	SUN XT	NA
VDDC	0.775~1.175V	0.775~1.125V	0.775~1.050V	0.775~1.000V	0.775~1.125V	0.800~1.075V	0.800~1.150V	NA
TDC	32A (TDC)	25A (TDC)	21A (TDC)	17A (TDC)	16A (TDC)	19A (TDC)	25A (TDC)	NA
EDC	48A	37.5A	31.5A	26A	24A	28.5A	37.5A	NA
OCP	57.6A	45A	37.8A	31.2A	28.8A	34.2A	45A	NA
Vboot	0.85V	0.85V	0.85V	0.85V	0.9V	0.9V	0.9V	NA
Load line	1mohm	1mohm	1mohm	---------	---------	---------	1mohm	NA
Ri PR860	1.13K Ohm	887 Ohm	750 Ohm	---------	---------	---------	887 Ohm	for OCP and LoadLine Setting
Rdroop PR842	1.43K Ohm	1.13K Ohm	953 Ohm	---------	---------	---------	1.13K Ohm	for LoadLine Setting
PR844	187K Ohm	147K Ohm	124K Ohm	---------	---------	---------	147K Ohm	for Compensation
PR847	51.1K Ohm	51.1K Ohm	51.1K Ohm	---------	---------	---------	51.1K Ohm	for Positive Offset

Remark: MARS LP/ SUN UL/ SUN PRO
don't use this 2-phase solution

H-side MOS:MDU1516
Rds(on):
9mohm@Vgs=10V
7.8~9mohm@Vgs=4.5V
Id :11A@Ta=25 degC

L-side MOS:UDU1511
Rds(on):
2.4mohm@Vgs=10V
2.7~3.3mohm@Vgs=4.5V
Id :24A@Ta=25 degC

Choke: 0.22uH (Size:7*7*4)
Rdc=0.98mohm +-5%
Heat Rating Current=28A
Saturation Current=28A

Remark:

1. PWM3 (Pin24) tie to 5V & CLK# (Pin40) external pull high
   => 2 phase CPU VR config
   PWM3 (Pin24) tie to 5V & CLK# (Pin40) tie to GND or floating
   => 2 phase GPU VR config

2. When 2 Phase GPU config
   a. DPSLPVR (Pin39)=0 PSI# (Pin2)=0
      =>1 phase CCM operation mode
   b. DPSLPVR (Pin39)=0 PSI# (Pin2)=1
      =>2 phase CCM operation mode
   c. DPSLPVR (Pin39)=1 PSI# (Pin2)=0 or 1
      =>1 phase DE operation mode

3. Rbias=147K =>overshoot reduction function disable
   Rbias=47k =>overshoot reduction function enable

4. Thermal throttling:
   Protect: (6.98K+Rth)*60uA=1.2V
   => Rth=13.02K
   =>Tp=110C (+-3C)
   Recovery:(6.98K+Rth)*56uA=1.24V
   => Rth=15.16K
   => Tr=105C (+-3C)

PR837=6.98K	PR837=1.5K
protect T 110C +-3	protect T 100C +-3
Recovery T 105C +-3	Recovery T 96C +-3

5. Switching frequency set :
   Rfset(kohm)=[period(us)-0.29]*2.65
   =5.9Kohm
   fsw=1/period(us)=400KHZ

20150129
unpop PC801 for lose dGPU issue

Module model information:
ISL62883C_V1A for IC
ISL62883C_V1B for SW Choke/MOS on BTN
ISL62883C_V2B for SW Choke on BTN, MOS on TOP

Layout Note:
PH801 should place near phase1 H-side MOS

Layout Note:
PH802 should place near Phase1 Choke

PR813 Pop:
for Loadline disable
PR813 @:
for Loadline enable and LL=1mohm

TDC 28A
Peak Current = 37.5A
OCP Current = 45A
Load line=1.1mohm

Transient response :
Rntcnet=(Rntcs+Rntc)*Rp/(Rntcs+Rntc+Rp)
Cn=L*(Rntcnet+Rsum/N)/[Rntcnet*DCR*(Rsum/N)]
N is the number of phases

Rdroop=Io*LL/Rdroop

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Title: ISL62883C

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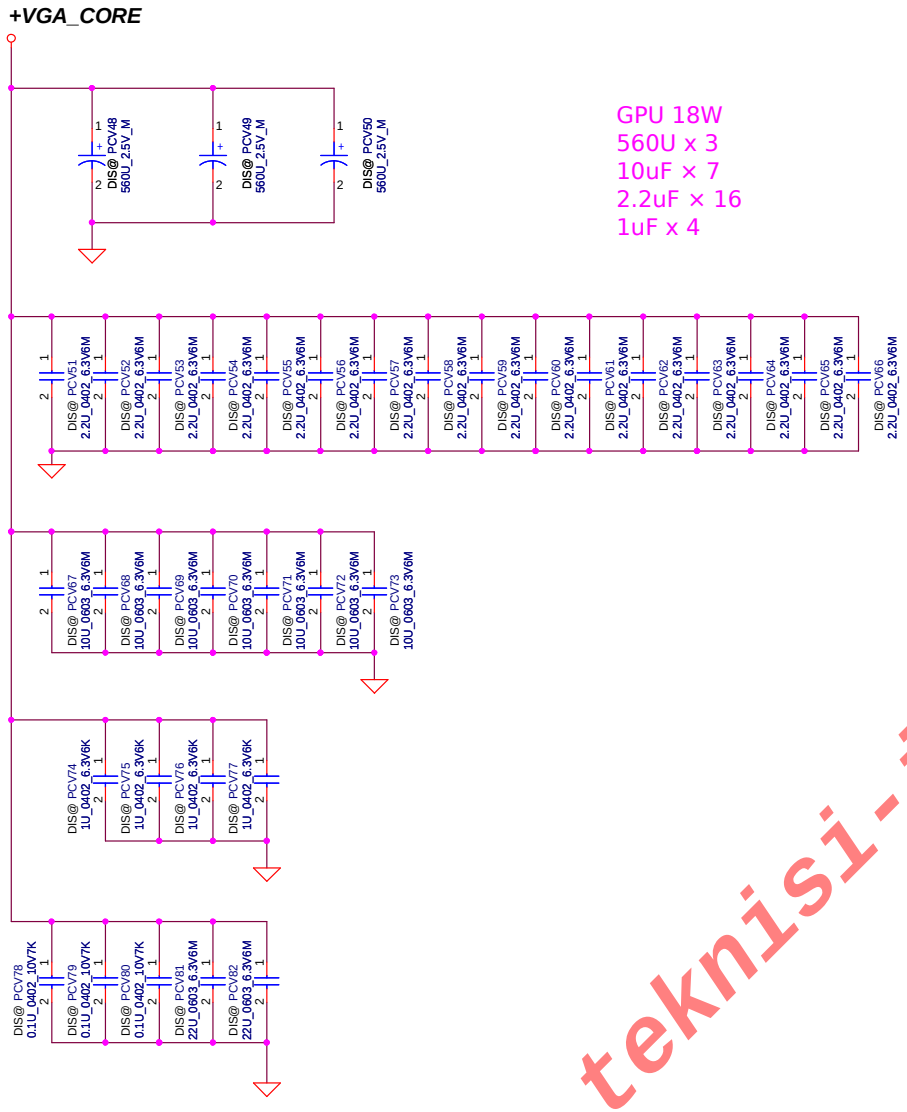

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Issued Date	2012/04/03	Deciphered Date	2016/09/30

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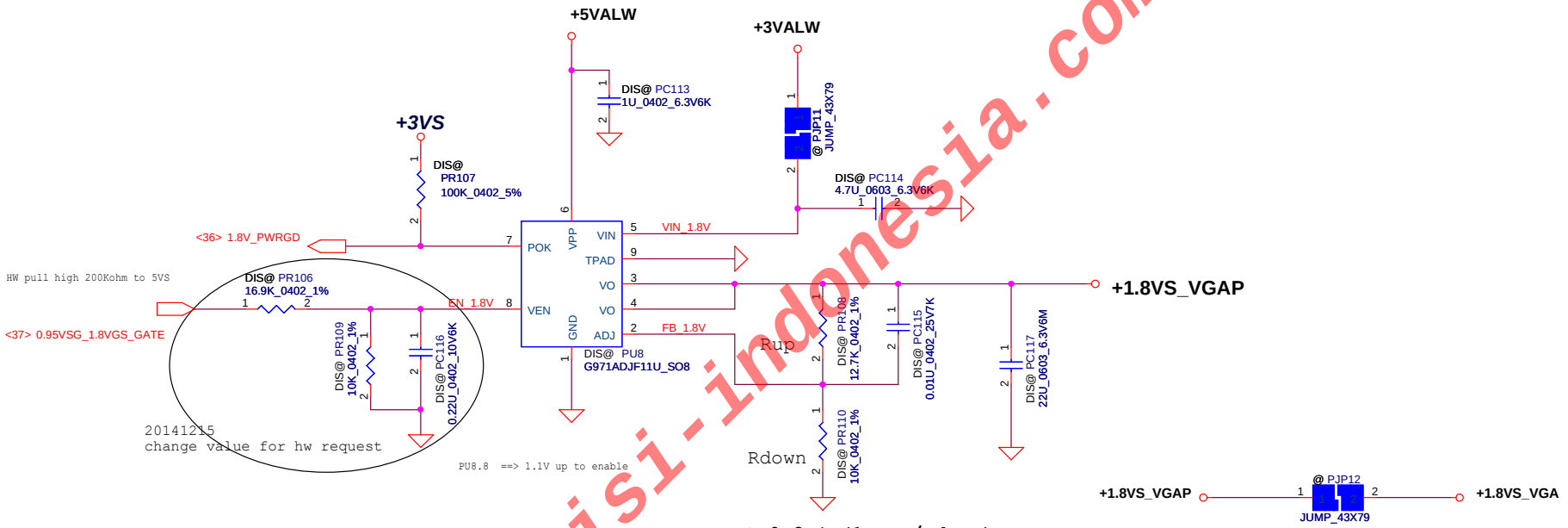

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Issued Date	2013/09/09	Deciphered Date	2016/09/30	Title: *+1.8VS_VGA*
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Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
1	change size		use common part for 7x7	change PL202 size from 10x10 to 7x7	SI
2	change part		no need 0ohm	PR224 and PR225 change from 0ohm to short pad	SI
3	change part		HW request	Change R, C value PR106 100k => 16.9k PR109 47k => 10k PC116 0.1U => 0.22U	SI
4	change part		Change PN	PC88 from SE000006OM8 to SE000006O00	PV
5	20150129		for lose dGPU issue	unmount PC801	PV

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Issued Date	Deciphered Date	Title: PIR List	
		Size: B	Document Number: LA-D703P	Rev: 0.1
		Date: Saturday, January 31, 2015	Sheet 58 of 60

Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
1	2014-11-25		A32 request	[A32] Reserve XDP circuit	DB
2	2014-11-25		A32 request	[A32] Reserve SMBUS from CPU to TP module	DB
3	2014-11-25	BDW CPU ESD issue	BDW CPU ESD issue solution	[Compal] Reserve Capx19 & Varistor x13 for BDW CPU ESD issue	DB
4	2014-11-25	[HP] Reserve XDP circuit	A32 request	[A32] eDP to VGA solution Sanrio--ITE IT6513 Candy--RTD2168	DB
5	2014-11-25		A32 request	[A32] KBC solution solution Sanrio--ENE KBC9012 Candy--ENE KBC9022	DB
6	2014-11-25		reduce component	[Compal] Remove WLAN LED circuit ,use KBC GPIO	DB
7	2014-11-25		A32 request	[A32] reserve TPM 1.2 & 2.0 TPM 1.2--SLB9665 TPM2.0--SLB9660	DB
8	2014-11-25		reduce component	[Compal] ODD load switch Sanrio use single load switch Candy use dual load switch	DB
9	2014-11-25		A32 request	[A32] Change WLAN connector Sanrio--mini card Candy--M.2 Conn	DB
10	2014-11-25		reduce component	[Compal] Sanrio use power switch for Fan control , Candy use PWM control from KBC	DB
11	2014-11-25		A32 request	[A32] Card reader solution Sanrio--RTS5239 Candy--RTS5141	DB
12	2014-11-25		A32 request	[A32] GPU solution Sanrio--Nvidia N15V-GM (17W) Candy--AMD Exo pro (18W)	DB
13	2014-11-25		reduce component	[Compal] +3VS to +3VS_VGA from dual load switch to single load switch +1.8VS_VGA power direct support	DB
14	2014-12-14		For LAN 1V regout	[Compal] Pop LL3	SI
15	2014-12-14		For fine turn DGPU power sequence	[Compal] Change C4122 value from 0,01u to 0.22u	SI
16	2014-12-14		For fine turn DGPU power sequence	[Compal] Change R4109 value from 200K to 6.98K	SI
17	2014-12-14		For fine turn DGPU power sequence	[Compal] Change C4109 value from 0,01u to 0.027u	SI
18	2014-12-14		Modify WLAN PCIE CLK request channel	[Compal] Modify WLAN CLK request channel from 2 to 5.	SI

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Title: **HW PIR List**

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Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
19	2014-12-14		Modify DGPU PCIE CLK request channel	[Compal] Modify DGPU CLK request channel from 3 to 4.	SI
20	2014-12-14		Modify LAN PCIE CLK request channel	[Compal] Modify LAN CLK request channel from 0 to 2.	SI
21	2014-12-23		HP request add thermal sensor for CPU PCB.	[Compal]Add CPU external Thermal sensor at EC_SMB_CK2/DA2.	SI
22	2014-12-23		CPU and GPU thermal sensor can't on the same bus.	GPU thermal sensor change to EC_SMB_CK3/DA3	SI
23	2014-12-23		Modify EC co-lay pin117 & 124.		SI
24	2014-12-24		EMI request to change HDMI schematic.		SI
25	2014-12-25		Reserved +5VS Touch power.		SI
26	2015-01-26		BIOS request.	Add pull-up at PCIECLKREQ1#	PV
27	2015-01-27		SVTP 3-9 fail.	R38 power change to +HDMI_CRT_5V , L7,L8,L9 change P/N.	PV
28	2015-01-27		SVTP 3-9 fail.	Remove Hsync,Vsync Buffer footprint.	PV
29	2015-01-28		Reserved for test.	Reserved 0 ohm on ODD_PLUG# , between CPU and ODD.	PV
210	2015-01-30		EMI request	Add 680p at PWR_LED#	

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